

# Optimal State Preparation for Logical Arrays on Zoned Neutral Atom Quantum Computers

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**Abstract**—Quantum computing promises to solve problems previously deemed infeasible. However, high error rates necessitate quantum error correction for practical applications. Seminal experiments with zoned neutral atom architectures have shown remarkable potential for fault-tolerant quantum computing. To fully harness their potential, efficient software solutions are vital. A key aspect of quantum error correction is the initialization of physical qubits representing a logical qubit in a highly entangled state. This process, known as state preparation, is the foundation of most quantum error correction codes and, hence, a crucial step towards fault-tolerant quantum computing. Generating a schedule of target-specific instructions to perform the state preparation is highly complex. First software tools exist but are not suitable for the zoned neutral atom architectures. This work addresses this gap by leveraging the computational power of SMT solvers and generating minimal schedules for the state preparation of logical arrays. Experimental evaluations demonstrate that actively utilizing zones to shield idling qubits consistently results in higher fidelities than solutions disregarding these zones. The complete code is publicly available in open-source as part of the *Munich Quantum Toolkit* (MQT) at <https://github.com/cda-tum/mqt-qmap>.

## I. INTRODUCTION

Quantum computing has emerged as a promising technology for solving computationally intensive tasks [1]. However, one major challenge is the high error rates in quantum devices. Although further advancements in physical implementations are expected to reduce these error rates, it is widely understood that practical quantum computations must always be fault-tolerant [2]. To this end, we can leverage the well-developed theory of *Quantum Error Correction* (QEC, [3]–[6]).

In QEC, a *logical qubit*, i. e., a qubit on the algorithmic level, is redundantly encoded into an array of *physical qubits*, a so-called *logical array*. One crucial part of QEC is preparing the physical qubits in a shared state representing the initial state of the encoded logical qubit before the actual algorithm can be executed. This process is known as *state preparation*. For many QEC codes, a circuit to perform the state preparation can be generated [7] and has then to be translated into a schedule of target-specific instructions.

By design, implementing QEC requires significantly more physical qubits than qubits at the logical level. However, as quantum devices continue to scale up in their qubit count [8], the application of QEC is finally becoming increasingly feasible. In experiments, researchers have already demonstrated the preparation of 40 logical qubits in the  $|0\rangle_L$ -state comprising 280 physical qubits using a *zoned neutral atom architecture*, where different operations are performed in designated spatially

separated zones [9]. Consequently, we urgently need appropriate software tools that automate the task of translating a state preparation circuit into a schedule of instructions specific to this quantum device.

For this highly complex task, we propose to use *Satisfiability Modulo Theories* (SMT) solvers [10]—a powerful and established method in traditional design automation—and apply them to the problem of compiling for zoned neutral atom architectures. The resulting approach allows the generation of *minimal* schedules in terms of the number of error-prone and time-intensive operations—crucial to achieving high fidelity.

Experimental evaluations show that the proposed approach consistently achieves higher fidelities than solutions that do not exploit the benefits of the zoned architecture. We extend those results by exploring different variations of the existing zoned neutral atom architecture, which provides valuable insights for the design of future quantum devices. The full code of the proposed approach is publicly available as part of the *Munich Quantum Toolkit* (MQT, [11]) at <https://github.com/cda-tum/mqt-qmap>.

## II. BACKGROUND

In order to keep the paper self-contained, this section provides (1) a brief review of the basics of QEC with a focus on state preparation as well as (2) an overview of neutral atom architectures.

### A. Quantum Error Correction and State Preparation

Qubits and quantum operations are inherently noisy due to their susceptibility to environmental influences and control errors. In order to prevent error accumulation and to enable large-scale quantum computations, several QEC protocols have been developed over the past decades [3]–[6]. Similar to classical error correction, the fundamental principle of QEC is to redundantly encode the information of one or more *logical qubits* into an array of *physical qubits*, a so-called *logical array*. A code that requires  $n$  physical qubits to encode  $k$  logical qubits with *code distance*  $d$ —the minimum number of physical errors that can lead to a logical error—is denoted as an  $[[n, k, d]]$  code.

The most common QEC codes are *Stabilizer Codes* [4]. Here, the logical qubit is encoded in the  $+1$ -eigenspace of a set of  $n - k$  linear independent Pauli operators (*stabilizers*) of the form  $P^{\otimes n}$ , where each entry  $P \in \{I, X, Y, Z\}$  represents a Pauli operator acting on a single qubit. This constraint reduces the  $2^n$  dimensional Hilbert space to the  $2^k$  dimensional *codespace* for the logical qubits.

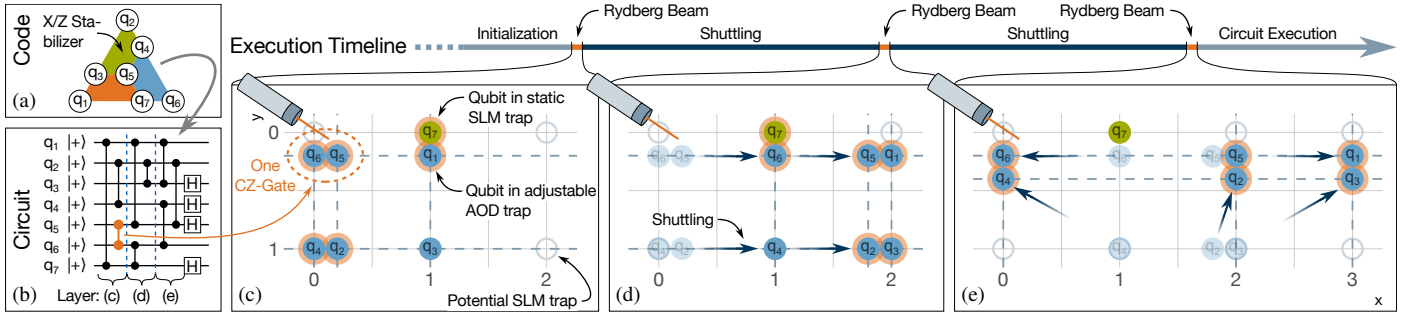


Figure 1. The visualization of the stabilizers of the Steane code (Fig. 1a) and a quantum circuit preparing the logical  $|0\rangle_L$ -state for this code (Fig. 1b). In the remaining part, a sequence of three Rydberg beams with intermediate shuttling indicated by the dark blue arrows realizing the circuit on the left. Each frame (Figs. 1c to 1e) corresponds to one layer of CZ-gates (separated by the barriers) in the circuit on the left.

**Example 1.** Fig. 1a illustrates the Steane code, a  $[[7, 1, 3]]$  code, which is the smallest instance of a 2D color code [5]. Circles represent physical qubits, and each of the three facets (green, blue, orange) defines two stabilizers: One with Z-operators and one with X-operators, acting on all qubits at the vertices of the facet, while identity operators act on the rest. This results, e. g., in the stabilizers  $IZZZZII$  and  $IXXXXII$  for the green facet.

Using QEC, the state  $|\psi\rangle_L$  of a logical qubit can be repeatedly checked for errors and corrected involving *syndrome extraction*, *decoding*, and *Pauli frame tracking* [4], [12]. However, before correction or computation, the state must be prepared as a valid logical state within the codespace. This process, known as *state preparation* (or *logical encoding*), involves a *state preparation circuit* that operates on the physical qubits.

Various methods have been proposed to design efficient state preparation circuits for different QEC codes. These include optimal schemes [13], heuristic approaches such as the "Latin rectangle" method [6], and machine learning techniques based on reinforcement learning [7].

**Example 2.** Fig. 1b shows a state preparation circuit for the Steane code. The physical qubits are initialized in the  $|+\rangle$  state followed by a series of CZ-gates and Hadamard gates at the end on selected qubits.

### B. Neutral Atom Architecture

Over time *neutral atoms* [14]–[18] have emerged as a promising platform for large-scale, fault-tolerant quantum computations [9]. Here, qubits are encoded in the electronic states of individual neutral atoms such as Rb, Sr, or Yb, which are trapped in optical tweezers and laser-cooled to their motional ground state [19].

Single-qubit gates are realized as state transitions driven by global and local lasers [14], [18]. Multi-qubit gates are implemented using the Rydberg blockade [18], [20]. Global Rydberg beams illuminate the entire trap area, enabling multiple parallel CZ-gates between all adjacent qubits. Isolated atoms, however, undergo an imperfect identity operation as they are still excited to the Rydberg state, suffering from Rydberg decay, which is a major error source for CZ-gates [20].

**Example 3.** Fig. 1c illustrates the application of a global Rydberg beam, performing the first three parallel CZ-gates of the circuit in Fig. 1b, i. e., between the pairs of qubits  $(q_1, q_7)$ ,  $(q_6, q_5)$ , and  $(q_4, q_2)$ . Qubit  $q_3$  is isolated and does not participate in any CZ-gate.

For the application of multi-qubit gates, their operands must be brought in proximity to each other. This is achieved by rearranging the atoms during computation—allowing for arbitrary qubit connectivity [18]. Experimentally, this is realized using two types of optical traps: (1) *Spatial Light Modulator* (SLM) traps, which define single static trap sites and (2) *Acousto-Optic Deflector* (AOD) traps, which create adjustable trap sites at crossings of perpendicularly intersecting AOD lines [18], [21]. An atom can be transferred from SLM to AOD traps and vice versa—called *loading* and *storing*, respectively—by activating or deactivating one AOD line crossing the atom [18], [21]. All atoms on the (de-)activated AOD line perform the same operation simultaneously, and unintended operations on other qubits must be carefully avoided [18], [22]. Loaded atoms are shuttled by moving AOD rows and columns whose order must be preserved [17].

**Example 4.** In Fig. 1c, qubit  $q_7$  is placed in an SLM trap (green), while the other qubits  $q_1, \dots, q_6$  are loaded in AOD traps (blue) in a 2D grid formed by two rows and three columns (dashed lines). Here, qubits  $q_4, q_2$ , and  $q_3$  share the same AOD row. Turning off this row would store all three qubits back into SLM traps. In Fig. 1d, the AOD columns are moved to the right, shuttling the AOD qubits (blue) indicated by the dark blue arrows relative to the static SLM qubit  $q_7$  (green). In total, the steps in Figs. 1c to 1e execute the state preparation circuit for the Steane code, depicted in Fig. 1b.

In order to execute entire quantum circuits, multiple steps of Rydberg beams and shuttling—potentially involving trap transfers—must take turns. Finding minimal schedules is crucial to compiling for neutral atom architectures [17]. Several tools have been proposed, including optimal solutions [23], [24], scalable heuristics [25]–[27], and combinations of shuttling with alternative routing methods [28], [29]. However, they all lack support for the novel *zoned* neutral atom architectures.

### III. CONSIDERED PROBLEM

A huge problem with state-of-the-art state-preparation for neutral atoms is that the Rydberg beams applied to execute CZ-gates affect not only the desired qubits but also the idling qubits. For example, during the step, illustrated in Fig. 1c, qubit  $q_3$  is illuminated by the Rydberg beam even though it is not involved in any CZ-gate. In order to avoid this unnecessary error source by the faulty identity operation, the Rydberg beam

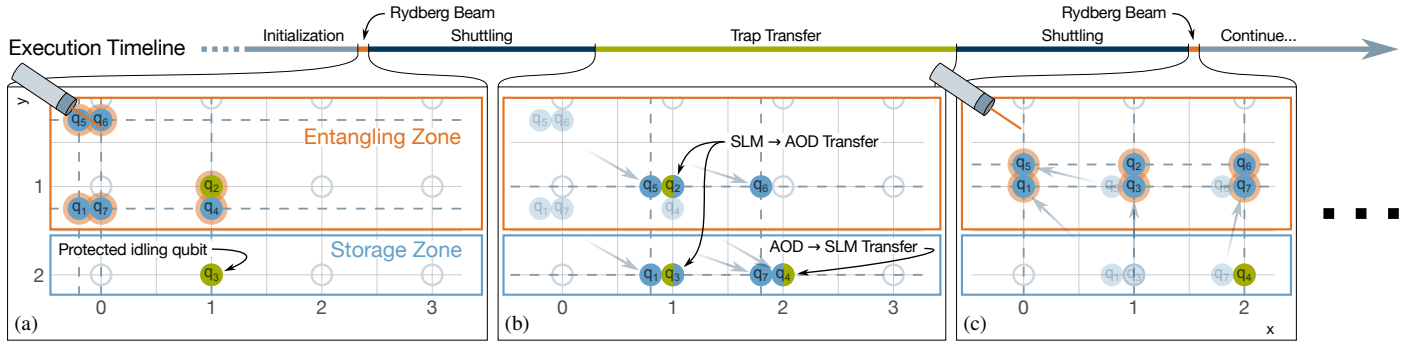


Figure 2. The first three steps of a schedule executing the same circuit as in Fig. 1b on a zoned neutral atom architecture. Throughout the two Rydberg beams shown in Figs. 2a and 2c, qubits  $q_3$  and  $q_4$ , respectively, are protected in the storage zone. Fig. 2b shows the necessary trap transfer.

should only illuminate qubits that undergo a CZ-gate. This is where *zoned* neutral atom architectures [9] come into play.

Here, the architecture is divided into spatially separated zones of three kinds: (1) *entangling zones*, where a global Rydberg beam can perform (entangling) CZ-gates between pairs of adjacent qubits, (2) *storage zones*, in which qubits are shielded from interferences with the Rydberg beam and where the qubits can be kept for a long time with very high coherence (single-qubit gates can be performed here as well), and (3) *readout zones*, in which selected qubits can be measured without collapsing the state of qubits in other zones.<sup>1</sup>

**Example 5.** Fig. 2a shows a schematic drawing of a zoned neutral atom architecture. While applying the Rydberg beam, qubit  $q_3$  is shielded in the storage zone. For the next Rydberg beam as in Fig. 2c, the qubits  $q_3$  and  $q_4$  have to be swapped. This swapping is no longer possible with shuttling alone and requires trap transfers as illustrated in Fig. 2b, where qubit  $q_4$  is stored in the storage zone and qubits  $q_3$  and  $q_2$  are loaded.

The required trap transfers take about 100 times longer than other operations on this architecture [9], [20]. Hence, their use should be minimized to the absolute minimum.

Both aspects—the consideration of different zones and the demand-driven use of transfers—are challenges not supported by existing tools reviewed in Sec. II. Those tools only assume a single zone (that corresponds to the entangling zone), including all unavoidable error sources. An exception are the compilers proposed in [22], [30], which can handle zoned architectures. However, the former cannot lead to minimal schedules as qubits are moved outside the entangling zone after every operation. The latter is designed for routing entire logical arrays and assumes that these arrays (representing logical qubits) have already been prepared. As such, the crucial state preparation step is missing.

In this work, we generate minimal schedules of target-specific instructions to perform the state preparation of logical arrays indispensable for most QEC codes. The circuits for the state preparation of arbitrary stabilizer codes can be expressed following the same structure as the circuit in Fig. 1b, i. e., first, the physical qubits are prepared in the  $|+\rangle$ -state, then a set of CZ-gates create a so-called *graph state*, and finally, the logical qubit is prepared in the  $|0\rangle_L$ -state by applying Hadamard gates on selected qubits [31]. Since the preparation of the physical

<sup>1</sup>Throughout the rest of this work, we will only consider storage and entangling zones. The treatment of readout zones can be handled analogously.

qubits in the  $|+\rangle$ -state, as well as the Hadamard gates at the end, can be realized everywhere on the architecture by rotational gates and does not require shuttling, this gives rise to the following problem statement:

**Problem.** Given a set of CZ-gates, find a schedule of Rydberg beams, trap transfers, and shuttling operations that realizes the given CZ-gates on the zoned neutral atom architecture with high fidelity.

#### IV. PROPOSED SOLUTION

In this work, we tackle the complexity of the problem reviewed above by utilizing the computational power of SMT solvers [10]. They are a powerful and established method from the conventional design automation realm and, as we show in the following, are well-suited for tackling problems arising in the compilation of quantum computing. The main idea is as follows: First, all possible schedules are represented symbolically, i. e., through a set of variables that represents, e. g., qubit positions, shuttling operations, and gate execution—leading to a *symbolic formulation* representing the entire search space. Then, constraints and an objective function are employed to ensure (1) those variables can only assume values corresponding to valid solutions and (2) that the solution is optimal. Finally, the resulting formulation is passed to an SMT solver trying to determine such an assignment. Naturally, the complexity of the problem remains, but as shown later in Sec. V, the proposed solution still facilitates the creation of schedules for practical instances. Even if the solver fails due to the complexity, it may still produce a valid assignment (cf. (1)), albeit not an optimal one (cf. (2)). From this assignment, the desired schedule can eventually be derived. The following sections describe the construction of the symbolic formulation, the constraints, and the objective function that encode the problem under consideration.

##### A. Symbolic Formulation

To ease the proposed formalization, we divide the time into discrete stages, and the space into finitely many trap sites, inspired by the model proposed in [24]. Those trap sites are grouped hierarchically into *interaction sites*. Each interaction site comprises one SLM trap in its center and potential AOD traps around it. At the beginning of a stage, each qubit is in one of these traps. Hence, its position is defined by the  $x$ - and  $y$ -coordinates of its interaction site together with the horizontal and vertical offset from the center within the interaction site.

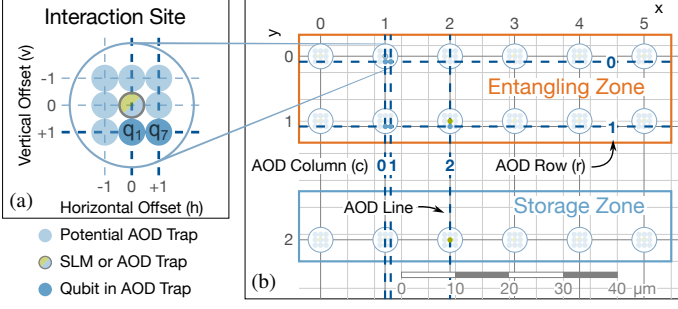


Figure 3. Schematic zoned neutral atom architecture with one storage zone corresponding to  $X_{\max} = 5$ ,  $Y_{\max} = 2$ ,  $H_{\max} = V_{\max} = 1$ ,  $C_{\max} = 2$ ,  $R_{\max} = 1$  and  $E_{\min} = 0$ ,  $E_{\max} = 1$ . In the center of each interaction site is an SLM trap surrounded by potential AOD traps.

Additionally, to allow only as many AOD columns and rows as the architecture can provide (and to facilitate the verification of AOD constraints [22]), qubits in AOD traps are assigned to their respective AOD column and row. For the rest of the paper, the letter  $q$  refers to a qubit, and the letter  $t$  denotes a stage.

**V1 (Positioning Qubits).**

$$\forall_{q,t} 0 \leq x_t^{(q)} \leq X_{\max}, \quad 0 \leq y_t^{(q)} \leq Y_{\max} \quad (1)$$

$$\forall_{q,t} |h_t^{(q)}| \leq H_{\max}, \quad |v_t^{(q)}| \leq V_{\max} \quad (2)$$

$$\forall_{q,t} a_t^{(q)} \in \{\text{true}, \text{false}\} \quad (3)$$

$$\forall_{q,t} 0 \leq c_t^{(q)} \leq C_{\max}, \quad 0 \leq r_t^{(q)} \leq R_{\max} \quad (4)$$

Eqs. (1) and (2) ensure that the  $x$ - and  $y$ -coordinates and the offset for each qubit are within the bounds of the architecture. The variable in Eq. (3) determines whether a qubit is loaded in an AOD trap; Eq. (4) limits the number of available AOD columns and rows.

**Example 6.** Fig. 3b illustrates a zoned architecture with an entangling zone and storage zone. A coordinate system spans the plane, identifying each interaction site with its  $x$ - and  $y$ -coordinates. Fig. 3a details the interaction site at  $x = 1$  and  $y = 0$ , showing the trap sites' possible horizontal and vertical offsets. Hence, for the qubit  $q_7$  this results, e. g., in the following variable assignment at stage  $t = 1$ :  $y_1^{(q_7)} = 0$ ,  $x_1^{(q_7)} = h_1^{(q_7)} = v_1^{(q_7)} = 1$ . In Fig. 3b, AOD lines (dashed blue lines) carry their index as a label, resulting in  $c_1^{(q_7)} = 1$ ,  $r_1^{(q_7)} = 0$ , and  $a_1^{(q_7)} = \text{true}$ .

There are two different kinds of stages: *Execution stages* and *transfer stages*. An execution stage starts with a Rydberg beam that causes CZ-gates between adjacent qubits, followed by shuttling the qubits to their position in the next stage. At the beginning of a transfer stage, qubits can transfer from static SLM to adjustable AOD traps and vice versa, followed by the shuttling of qubits to their subsequent position.

We assume that the CZ-gates constituting the state preparation circuit are given as a list  $\langle g_1, \dots, g_G \rangle$  of (unordered) pairs of qubits. Later, we need to refer to the (unordered) pair of operands itself, which we denote as  $\text{im}(g_i)$  for some  $i \in [G]$ , where  $[G] := \{1, \dots, G\}$ .

**V2 (Executing Gates).**

$$\forall_{i \in [G]} 0 \leq g_i < S \quad (5) \quad \forall_t e_t \in \{\text{true}, \text{false}\} \quad (6)$$

The constant  $S$  is an input parameter and denotes the total number of stages, and hence Eq. (5) ensures that all gates are executed within the given number of stages. The variable in Eq. (6) determines whether a stage is an execution stage or not. **Example 7.** Note that Fig. 3 extends the step depicted in Fig. 1c. The corresponding stage is an execution stage where the first three CZ-gates of the circuit in Fig. 1b are executed, i. e.,  $g_i = 1$  if  $i = 1, 2, 3$  else  $g_i \neq 1$  and  $e_1 = \text{true}$ .

Qubits can be transferred from static SLM to adjustable AOD traps and vice versa, which is called *loading* and *storing*, respectively. To avoid unintended load and store operations, we label every AOD column and row that is responsible for a load or store operation accordingly.

**V3 (Loading/Storing Qubits).**

$$\forall_{k \in \{0, \dots, C_{\max}\}, t} c_{l_t}^{(k)}, c_{s_t}^{(k)} \in \{\text{true}, \text{false}\} \quad (7)$$

$$\forall_{k \in \{0, \dots, R_{\max}\}, t} r_{l_t}^{(k)}, r_{s_t}^{(k)} \in \{\text{true}, \text{false}\} \quad (8)$$

In Eq. (7), when a variable has the value `true` for a column, then all qubits in this column must be loaded or stored (in that stage), respectively; the same holds for rows in Eq. (8), analogously.

**Example 8.** For stage  $t = 2$ , depicted in Fig. 1d,  $c_{l_2}^{(1)}$  and  $c_{s_2}^{(2)}$  are `true` whereas all other variables from Box V3 are `false`. This reflects that all qubits previously on column 1 are stored, and qubits afterward on column 2 are loaded.

**B. Constraints**

Most of the possible assignments are invalid because they describe physically infeasible schedules. To limit the search space to assignments that describe valid solutions, we introduce constraints on the variables to reflect the restrictions imposed by the neutral atom architecture. Most obviously, a trap can hold at most one qubit at a time.

**C1 (Positioning Qubits).**

$$\forall_{t, q, q'} \left( h_t^{(q)} = h_t^{(q')} \right) \wedge \left( v_t^{(q)} = v_t^{(q')} \right) \rightarrow \left( x_t^{(q)} \neq x_t^{(q')} \right) \vee \left( y_t^{(q)} \neq y_t^{(q')} \right) \quad (9)$$

$$\forall_{q,t} \neg a_t^{(q)} \rightarrow \left( h_t^{(q)} = 0 = v_t^{(q)} \right) \quad (10)$$

Eq. (9) requires qubits with identical horizontal and vertical offsets to be located at different interaction sites, implying that two qubits can never be at the same position. As only the center qubit in an interaction site can be confined in an SLM trap, such a qubit must have zero offsets, cf. Eq. (10).

AOD traps are created at crossings of AOD columns with rows. For a consistent model, we arrange the columns from left to right in increasing order. Analogously, there is a constraint for the rows, which is omitted for brevity.

**C2 (Ordering AOD lines).**

$$\forall_{q, q', t} \left( a_t^{(q)} \wedge a_t^{(q')} \right) \rightarrow \left( c_t^{(q)} < c_t^{(q')} \leftrightarrow x_t^{(q)} < x_t^{(q')} \vee \left( x_t^{(q)} = x_t^{(q')} \wedge h_t^{(q)} < h_t^{(q')} \right) \right) \quad (11)$$

At the beginning of an execution stage, all qubits in the entangling zone in proximity to each other undergo a CZ-gate.

Central to our work is the utilization of the different zones provided by the architecture. Idling qubits are moved outside the entangling zone to be shielded from the Rydberg beam.

**C3 (Executing Gates).**

$$\forall_{i \in [G]} (g_i = t) \rightarrow \left( e_t \wedge \left( x_t^{(q)} = x_t^{(q')} \right) \wedge \left( y_t^{(q)} = y_t^{(q')} \right) \right. \\ \left. \wedge \left( \left| h_t^{(q')} - h_t^{(q)} \right| < r \right) \wedge \left( \left| v_t^{(q')} - v_t^{(q)} \right| < r \right) \right) \quad (12)$$

$$\wedge \left( E_{\min} \leq y_t^{(q)} \leq E_{\max} \right) \wedge \left( E_{\min} \leq y_t^{(q')} \leq E_{\max} \right)$$

$$\forall_{i, j \in [G]} (g_i \neq g_j) \quad \text{if} \quad \text{im}(g_i) \cap \text{im}(g_j) \neq \emptyset \quad (13)$$

$$\forall_q e_t \rightarrow \neg \left( \left( \forall_{i \in [G]} g_i \neq t \right) \wedge \left( E_{\min} \leq y_t^{(q)} \leq E_{\max} \right) \right) \quad (14)$$

For a gate  $g_i$  to be executed in stage  $t$ , Eq. (12) ensures that all prerequisites are fulfilled such that the gate is physically executed. Gates involving the same qubits cannot be executed simultaneously, cf. Eq. (13). The constants  $E_{\min}$  and  $E_{\max}$  are the bounds of the entangling zone, and hence, Eq. (14) enforces the shielding of idling qubits—vital to achieving high fidelity.

Apart from constraints validating the configuration at the beginning of each stage, further constraints are required to relate successive stages. In an execution stage, only rearranging the qubits is allowed, but no trap transfers are allowed.

**C4 (Shuttling in Execution Stage).**

$$\forall_{q,t} e_t \rightarrow \left( a_t^{(q)} = a_{t+1}^{(q)} \right) \quad (15)$$

$$\forall_{q,t} e_t \rightarrow \left( a_t^{(q)} \vee \left( \left( x_t^{(q)} = x_{t+1}^{(q)} \right) \wedge \left( y_t^{(q)} = y_{t+1}^{(q)} \right) \right) \right) \quad (16)$$

$$\forall_{q,t} e_t \rightarrow \left( \neg a_t^{(q)} \vee \left( \left( c_t^{(q)} = c_{t+1}^{(q)} \right) \wedge \left( r_t^{(q)} = r_{t+1}^{(q)} \right) \right) \right) \quad (17)$$

Eq. (15) enforces the invariance of the trap's type. During shuttling, only qubits in AOD traps can move, cf. Eq. (16), but must stay on their column and row, cf. Eq. (17).

In contrast, transfer stages explicitly allow qubit transfers between trap types. First, qubits are stored.

**C5 (Storing in Transfer Stage).**

$$\forall_{q,t} \neg e_t \rightarrow \left( a_{t+1}^{(q)} \vee \left( h_t^{(q)} = 0 = v_t^{(q)} \right) \right) \quad (18)$$

$$\forall_{q,t} \neg e_t \rightarrow \left( a_{t+1}^{(q)} \vee \left( \left( x_t^{(q)} = x_{t+1}^{(q)} \right) \wedge \left( y_t^{(q)} = y_{t+1}^{(q)} \right) \right) \right) \quad (19)$$

$$\forall_{q,t} \neg e_t \rightarrow \left( \neg a_t^{(q)} \vee \left( \neg a_{t+1}^{(q)} \leftrightarrow c_{s_t}^{(q)} \vee r_{s_t}^{(q)} \right) \right) \quad (20)$$

The storing can only happen at the location of the SLM trap, i. e., with zero horizontal and vertical offset, cf. Eq. (18). Next, cf. Eq. (19) ensures that stored qubits and those in SLM traps remain at their position. The transfer of a qubit from an AOD to an SLM trap happens by ramping down the intensity of at least one of the AOD lines crossing the atom. Consequently, all qubits on this line must be stored, cf. Eq. (20).

The loading of qubits happens after the storing. Qubits in AOD traps and those loaded can subsequently shuttle to their next position. The following Eq. (21) ensures that after the transfer, the relative horizontal order of AOD qubits (loaded ones and those remaining in AOD traps) is maintained.

**C6 (Loading and Shuttling in Transfer Stage).**

$$\forall_{q,q',t} \left( \neg e_t \wedge a_{t+1}^{(q)} \wedge a_{t+1}^{(q')} \right) \rightarrow \left( \left( x_t^{(q)} < x_t^{(q')} \right) \vee \right. \\ \left. \left( \left( x_t^{(q)} = x_t^{(q')} \right) \wedge \left( h_t^{(q)} < h_t^{(q')} \right) \right) \leftrightarrow \left( c_{t+1}^{(q)} < c_{t+1}^{(q')} \right) \right) \quad (21)$$

The vertical order is analogously ensured by a constraint that is omitted for brevity. Similar to the store operation, i. e., Eq. (20), the loading operation is constrained similarly, which is also not shown here for brevity.

**C. Objective Function**

The presented constraints guarantee that satisfying assignments only lead to physically feasible schedules. However, there is no way to decide which of the possible schedules is the best. To this end, we introduce an objective function that determines the optimal solution.

As the execution time of a circuit increases, the probability of errors due to decoherence generally rises, resulting in decreased fidelity. Moreover, each Rydberg beam carries a certain probability of error. We optimize for both factors by seeking the schedule with the minimum overall number of stages  $S$ .

**V. EVALUATION**

The proposed approach is the first that provides a method for optimal state preparation on *zoned* neutral atom architectures. Experimental evaluations have been conducted to evaluate its applicability. This section reviews the considered setup and summarizes the obtained results, including a discussion of them.

**A. Setting**

In order to highlight the impact of utilizing the architecture's zones on the overall fidelity, we consider three different layouts: (1) *No Shielding*: one entangling zone without a storage zone, which implies that qubits cannot be shielded and which serves as a baseline<sup>2</sup>; (2) *Bottom Storage*: one storage zone below the entangling zone; and (3) *Double-Sided Storage*: storage zones on both sides of the entangling zone to see whether the extra storage zone can mitigate the additional shuttling overhead caused by shielding idling qubits.

In all cases, we assume that the entire architecture offers eight columns ( $X_{\max}=7$ ) and seven rows ( $Y_{\max}=6$ ), which are split into the zones for the respective layout such that a storage zone always has two rows. Accordingly, the entangling zone spans all rows in Layout 1 ( $E_{\min}=0, E_{\max}=6$ ), the five top rows in Layout 2 ( $E_{\min}=2, E_{\max}=6$ ), and the three middle rows in Layout 3 ( $E_{\min}=2, E_{\max}=4$ ). Further, we assume the architecture features six AOD lines in each direction ( $C_{\max}=R_{\max}=5$ ). We allow a relative offset in every direction of two ( $H_{\max}=V_{\max}=2$ ). For qubits to interact, their sites must either be directly or diagonally adjacent ( $r=2$ ).

To meet the objective function, we gradually increment the number of stages  $S$  until we find a satisfiable instance. To solve the individual instances we employ the Z3 solver [10]. The input circuits, following the same structure as the circuit in

<sup>2</sup>For this layout, the Eq. (14) is unsatisfiable and must be replaced with a constraint ensuring that idling qubits are sufficiently separated, i. e., sit in different interaction sites.

Table I. LAYOUT COMPARISON

Code	#CZ	(1) No Shielding				(2) Bottom Storage				(3) Double-Sided Storage			
		#R	#T	⊙	ASP	#R	#T	⊙	ASP	#R	#T	⊙	ASP
$[[7, 1, 3]]$ Steane	9	3	0	352.4	0.94	3	2	1562.3	0.94	3	1	1069.4	0.94
$[[9, 1, 3]]$ Surface	8	5	0	519.1	0.91	3	1	1154.8	0.94	3	0	493.9	0.95
$[[9, 1, 3]]$ Shor	10	3	0	656.0	0.82	5	3	2326.0	0.92	5	0	850.3	0.94
$[[15, 7, 3]]$ Hamming	28	7	0	759.8	0.59	7*	4*	2625.3*	0.82*	7*	2*	1942.9*	0.83*
$[[15, 1, 3]]$ Tetrahedral	28	7	0	808.1	0.59	7*	4*	3014.2*	0.82*	7*	2*	2179.2*	0.83*
$[[17, 1, 5]]$ Honeycomb	32	7	0	963.5	0.57	7*	5*	3002.4*	0.80*	7*	3*	2462.1*	0.81*

#CZ: Num. CZ-gates      #R: Num. Rydberg stages      #T: Num. transfer stages      ⊙: Schedule Exec. time [μs]      ASP: Approx. success prob.  
 \*Results may not be optimal due to solver's timeout after 320 h.

Fig. 1b, are generated by taking the stabilizers of popular QEC codes and applying the tool STABGRAPH [31].

For the assessment of the results, we employ the *Approximated Success Probability* (ASP) [17] as a proxy for the overall fidelity of the circuit. For a circuit with  $G$  gates, the ASP is defined by

$$\text{ASP} = \exp\left(-\frac{t_{\text{idle}}}{T_{\text{eff}}}\right) \cdot \prod_{i=0}^G \mathcal{F}_{g_i},$$

where  $t_{\text{idle}}$  is the accumulated idle time of all qubits,  $T_{\text{eff}} = 1$  s [9], and  $\mathcal{F}_{g_i}$  is the fidelity of the respective gate. The calculation of the ASP is based on the following figures of merit with  $\text{Id}_{\text{Ryd}}$  being the faulty identity operation affected by the Rydberg beam:

Operation	Fidelity $\mathcal{F}$	Duration [μs]	Speed [ $\frac{\mu\text{s}}{\mu\text{m}}$ ]
CZ/ $\text{Id}_{\text{Ryd}}$	0.995/0.998[20]	0.27[9]	–
local RZ	0.99912[9]	5 [9]	–
global RY	0.9999 [9]	1 [9]	–
Load/Store	0.999 [9]	200 [9]	–
Shuttling	1.0 [9]	–	0.55[18]

With respect to the shuttling distances, we assume that sites within one interaction site are separated by a distance of 1 μm, and entire interaction sites by 14 μm to safely avoid long-distance interactions between qubits sitting in neighboring interaction sites [9]. The zones are laid out such that qubits in different zones are at least 20 μm apart from each other [9].

### B. Obtained Results

Table I summarizes the results. Here, the first two columns denote the code and the corresponding number of CZ-gates needed to prepare the state. Then, the following columns provide the obtained results: #R and #T denote the number of Rydberg and transfer stages, respectively, ⊙ denotes the overall execution time it takes to perform the schedule on the neutral atom architecture, and ASP denotes the approximated success probability. The latter is the primary measure to compare different schedules. For Layouts 2 and 3, the difference in the ASP compared to Layout 1 is highlighted in Fig. 4. The higher the bar is, the more significant the respective improvement. Note that—despite the complexity—for the smaller codes, i. e., the first three, the solver terminates within hundreds of milliseconds; for the larger codes, however, it takes up to several days for individual SMT instances and in few cases we obtain results not guaranteed to be optimal due to timeout.

### C. Discussion

The results confirm that the proposed approach—for the first time—can generate minimal schedules for state preparation on the zoned neutral atom architecture. While the approach has scalability limitations, as expected due to the problem's inherent complexity, this is not a significant concern: the schedules only need to be generated once and can serve as optimal building blocks that are instantly usable during compilation.

The proposed approach also allows to evaluate the benefits of the *zoned* neutral atom architecture for the first time. In fact, Table I reveals consistently higher fidelities, reflected by the ASP, for Layouts 2 and 3 compared to Layout 1, which clearly shows the advantage of shielding idling qubits in the storage zone. The proposed approach achieves this advantage even in the cases where the results for Layouts 2 and 3 are not guaranteed to be optimal. Existing solutions do not account for zones, with all operations occurring implicitly in the entangling zone. As a result, their performance can only match, but never exceed, the figures presented for Layout 1.

Moreover, Fig. 4 shows that the ASP can further be improved by having storage zones on both sides of the entangling zone since shuttling distances are shorter and fewer transfer stages are required. These results provide valuable insights for the design of future quantum devices.

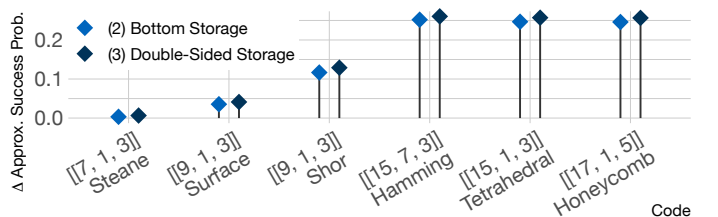


Figure 4. Differences in the ASP for different codes and layouts.

## VI. CONCLUSIONS

Zoned neutral atom architectures offer an excellent opportunity to shield idle qubits from interfering influences. However, so far, those architectures lack appropriate software support. In this work, we have proposed an SMT-based approach to generate minimal schedules for state preparation circuits tailored to this architecture. The evaluation demonstrates the benefits of the proposed technique for shielding idling qubits and for exploring different hardware design choices.

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