

informatik-Kolloquium

Der Fachbereich Informatik der Johannes Kepler Universität Linz¹ lädt in Zusammenarbeit mit der Österreichischen Gesellschaft für Informatik (ÖGI) zu folgendem Vortrag ein:

Topic: Formal methods for ranking verification counterexamples through assumption mining

Presenter: Ass.-Prof. Dr. Ansuman Banerjee
Indian Statistical Institute (ISI), Kolkata, India

Datum: Friday, February 23rd 2018, 10:00

Location: JKU, Computer Science Building (Science Park 3), room S3 058

Abstract:

Unit testing and verification constitute an important step in the validation life cycle of large and complex multi-component designs. Many unit validation methods often suffer from the problem of false negatives, when they analyze a component in isolation and look for errors. It often turns out that some of the reported unit failures are infeasible, i.e. the valuations of the component input parameters that trigger the failure scenarios, though feasible on the unit in isolation, cannot occur in practice considering the integrated design, in which the unit-under-test is instantiated. In this talk, we consider this problem in the context of a multi-component design, with a set of unit failures reported on a specific unit. We present an automated two-stage failure scenario classification and prioritization strategy that can filter out false negatives and cluster them accordingly. The use of classical artificial intelligence and program analysis techniques in conjunction with formal verification helps in developing new frameworks for reasoning and deduction, which appear promising for a wide variety of problems.

Short Bio:

Ansuman Banerjee is currently serving as an Associate Professor at the Advanced Computing and Microelectronics Unit, Indian Statistical Institute (ISI) Kolkata. His research interests include design automation for embedded systems, hardware-software verification, VLSI CAD, and automata theory. Ansuman received his Ph.D. from IIT Kharagpur.

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