





Der Fachbereich Informatik der Johannes Kepler Universität Linz<sup>1</sup> lädt in Zusammenarbeit mit der Österreichischen Gesellschaft für Informatik (ÖGI) zu folgendem Vortrag ein:

## Topic: Simulation and Verification of non-functional properties

Presenter: Dr. Pablo González de Aledo, Imperial College London

Datum: Tuesday, November 7<sup>th</sup> 2017, 08:30

Location: JKU, Computer Science Building (Science Park 3), room S3 048

**Abstract:** Unlike other generic computing systems, embedded real-time systems (ERTSs) interact with their environment and are subject to specific constraints; so their design usually faces particular challenges that are unique to this discipline. In these systems, the correctness of the design depends not only on the fact that it can compute something, but also on the fact that it can deliver a result before a certain deadline, with low energy consumption, requiring a minimal memory footprint, and in such a way that the thermal behavior of the chip does not degrade its functionality and reliability. These non-functional properties are as important as (or even more important than) the result of the computation per se. By "non-functional" properties, we refer to energy consumption, memory transactions, bus and NoC contention, memory optimization, load balancing, execution time, thermal behavior, etc. These non-functional properties are meant to induce longer battery life, smoother user interaction, better quality in the transmissions or more reliability. This talk presents various techniques and tools for tackling the design challenges that are unique to ERTSs. We propose to combine "native simulation", "symbolic execution" and "trace refinement" to analyze the non-functional properties of embedded systems and demonstrate that such combination advances the state of the art in the analysis and verification of embedded real-time systems.

**Short Bio:** Pablo González-de-Aledo received the telecommunications engineering degree from the University of Cantabria, Santander, Spain and holds a Ph.D. from the same university as well as the Department of Computing, Macquarie University, Sydney, NSW, Australia. He started his research career with the Network-on-Chip Team, ST-Microelectronics, Grenoble, France. After researching in the modeling and simulation of high-performance, multicore, and heterogeneous platforms for some European projects he became interested in the theory behind formal methods and worst-case-execution-time. He is currently working with Imperial College of London in adapting compiler technologies to increase the performance and energy efficiency of computer vision algorithms such as SLAM.

Einladender: Univ.-Prof. Dr. Robert Wille Institut für Integrierte Schaltungen Abteilung Integrierter Schaltungs- und Systementwurf

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