Connectivity Aware Synthesis of QuantumAlgorithms using the Parity Architecture

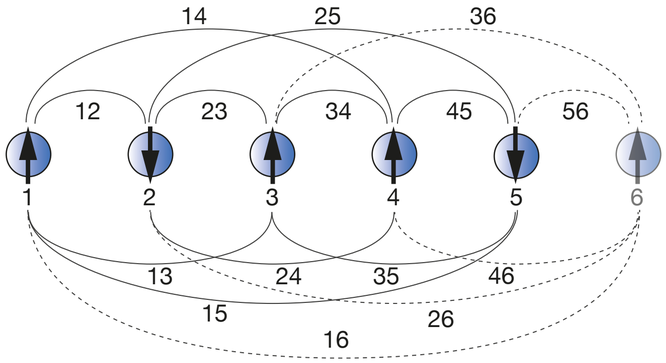
Munich Quantum Software Forum 2025

Wolfgang Lechner

21.October 2025

The Parity Transformation

W. Lechner., P. Hauke, and P. Zoller. *Sci. Adv.* ***1****, e1500838* (2015).



$$H = \sum_{i=1}^{N} \sum_{j=1}^{i} J_{ij} \sigma_{z,L}^{(i)} \sigma_{z,L}^{(j)}$$

- NP-hard optimization problems can be formulated as Ising Spin-glasses.

- This formulation requires high connectivity.

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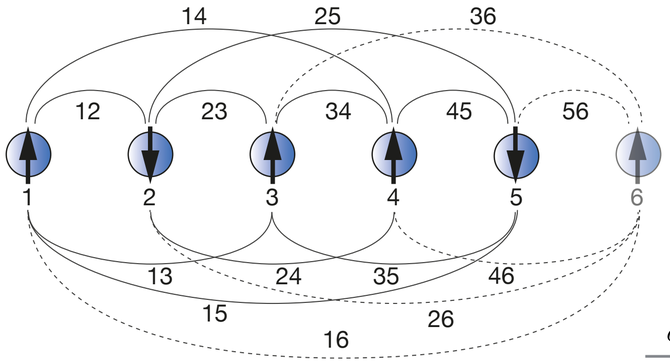

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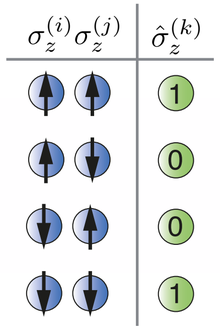

$$H = \sum_{i=1}^{K} J_i \sigma_z^{(i)}$$

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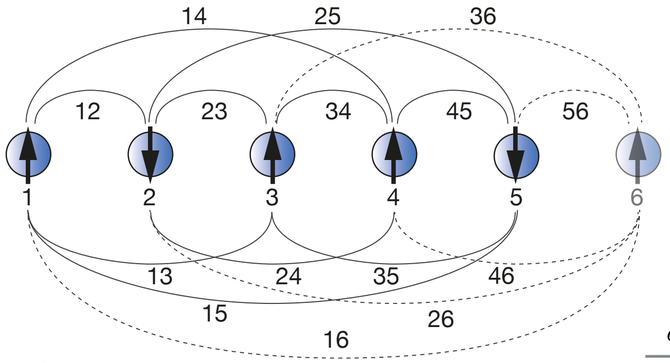
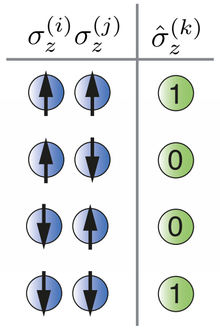


N *degrees of freedom*

$$H = \sum_{i=1}^{N} \sum_{j=1}^{i} J_{ij} \sigma_{z,L}^{(i)} \sigma_{z,L}^{(j)}$$



$$K = \frac{N(N-1)}{2}$$ *degrees of freedom*

$$H = \sum_{i=1}^{K} J_i \sigma_z^{(i)}$$

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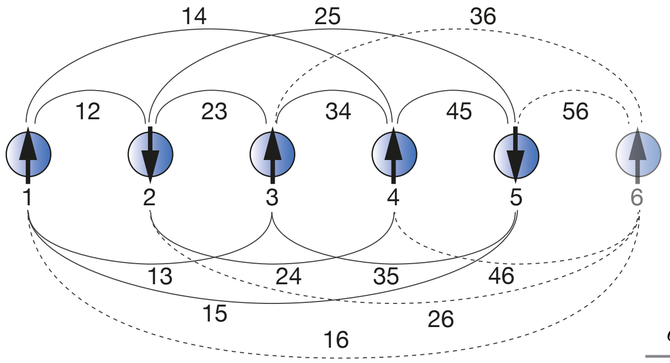

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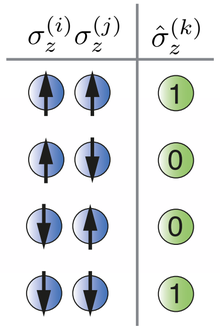

$$K = \frac{N(N-1)}{2}$$ *degrees of freedom*

$K - N + 1$ *constraints*

$$H = \sum_{i=1}^{K} J_i \sigma_z^{(i)} + \sum_{l=1}^{K-N+1} C_l$$

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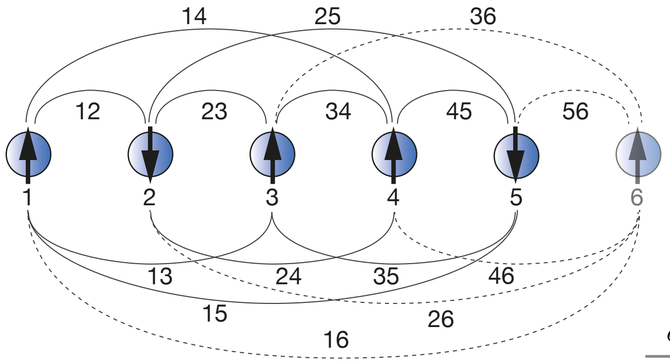

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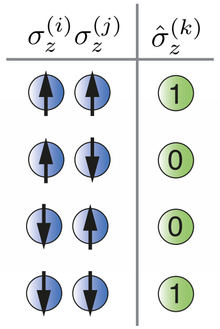

$$K = \frac{N(N-1)}{2} \quad \textit{degrees of freedom}$$

$$K - N + 1 \quad \textit{constraints}$$

$$H = \sum_{i=1}^{K} J_i \sigma_z^{(i)} + \sum_{l=1}^{K-N+1} C_l \qquad C_l = -c_l \sigma_z^{(l_1)} \sigma_z^{(l_2)} \sigma_z^{(l_3)} \sigma_z^{(l_4)}$$

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What are these constraints?

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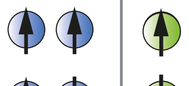
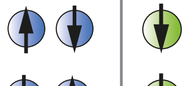
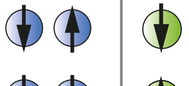
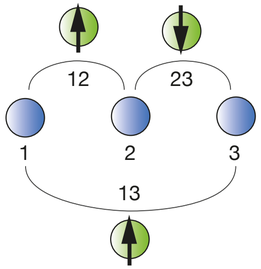
Conditions on closed loops

$\sigma_z^{(i)}\sigma_z^{(j)}$	$\hat{\sigma}_z^{(k)}$
	
	
	
	



$\sigma_z^{(1)}$	$\sigma_z^{(2)}$	$\sigma_z^{(3)}$	$\hat{\sigma}_z^{(12)}$	$\hat{\sigma}_z^{(13)}$	$\hat{\sigma}_z^{(23)}$
0	0	0	0	0	0
1	1	1	0	0	0
1	1	0	0	1	1
	...			...	
~~0~~	~~0~~	~~1~~	0	0	1

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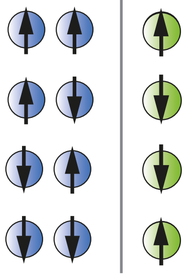	

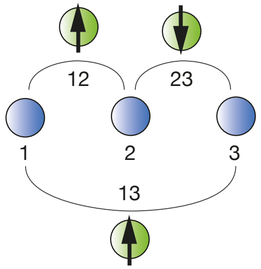

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0	0	0	0	0	0
1	1	1	0	0	0
1	1	0	0	1	1
	...			...	
~~0~~	~~0~~	~~1~~	0	0	1

In **each closed loop**, the number of **spins down** has to be an **even** number or 0.

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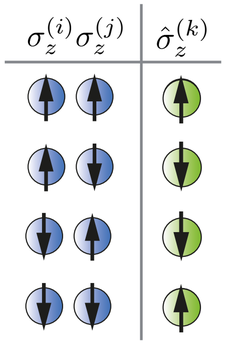

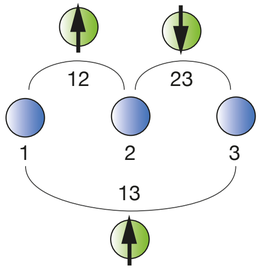

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0	0	0	0	0	0
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	…			…	
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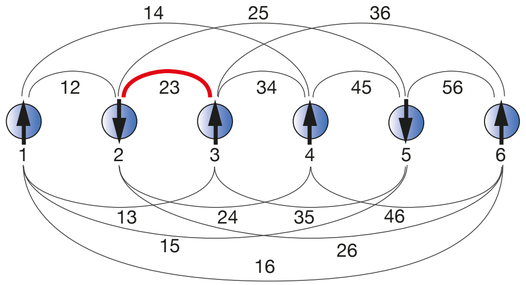

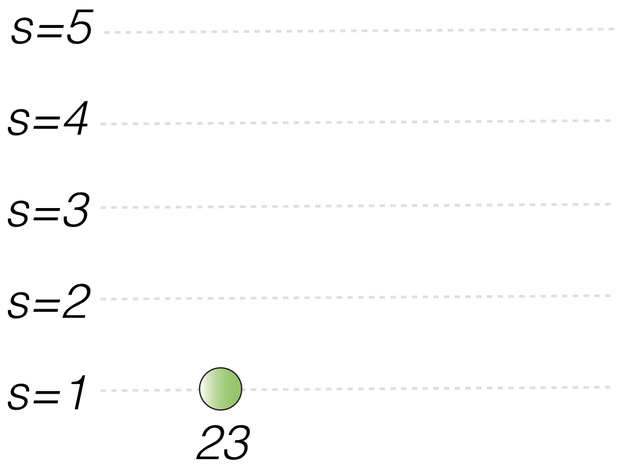

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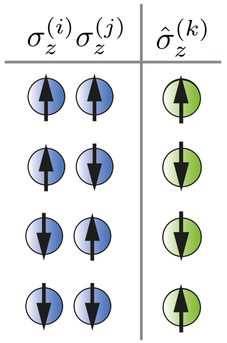

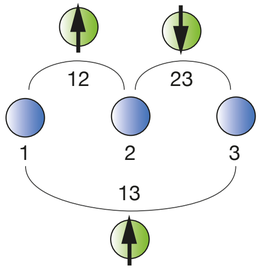

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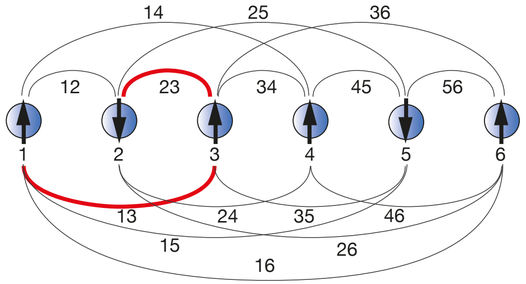

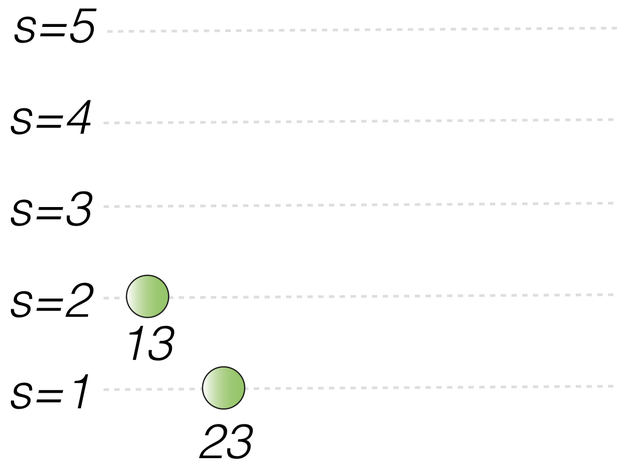

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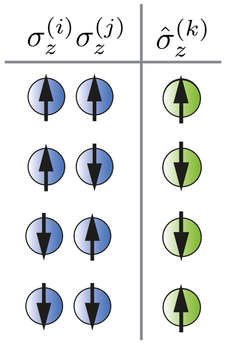

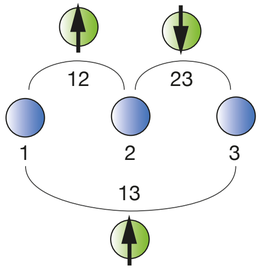

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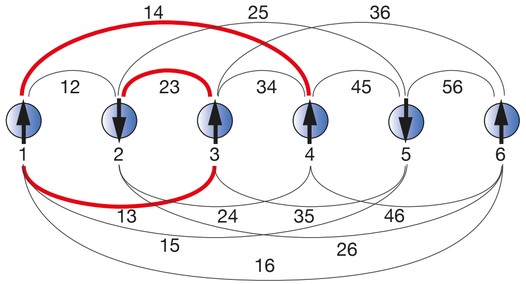

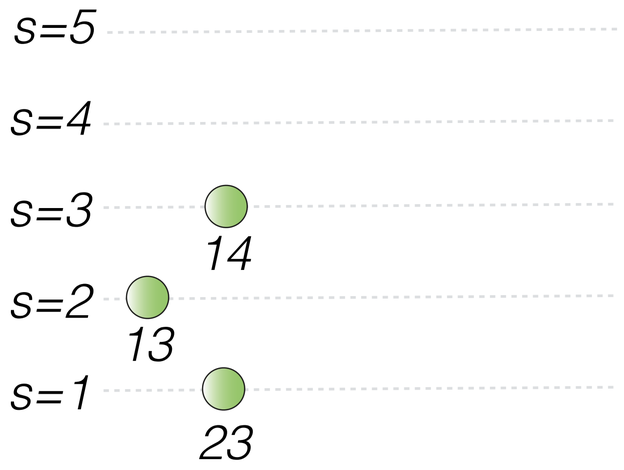

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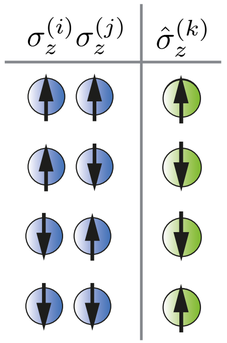

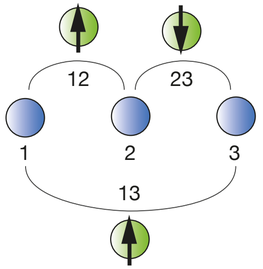

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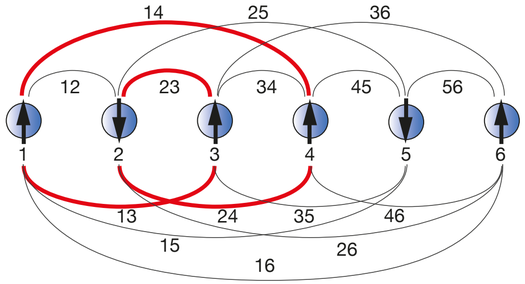

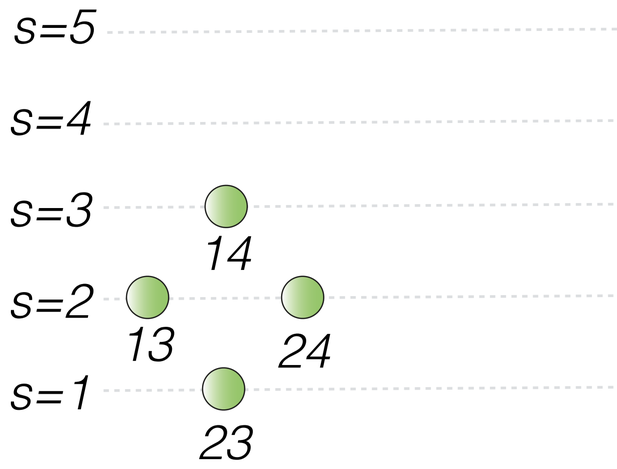

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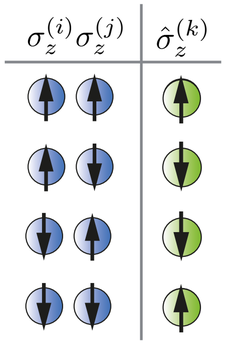

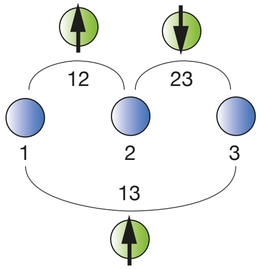

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0	0	0	0	0	0
1	1	1	0	0	0
1	1	0	0	1	1
	...			...	
~~×~~	~~×~~	~~×~~	0	0	1

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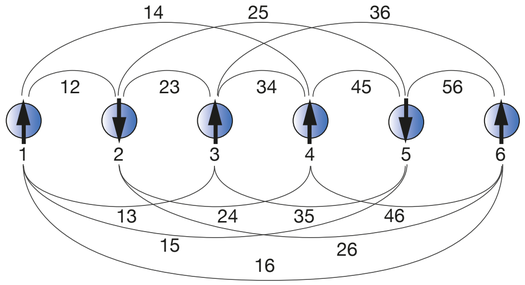

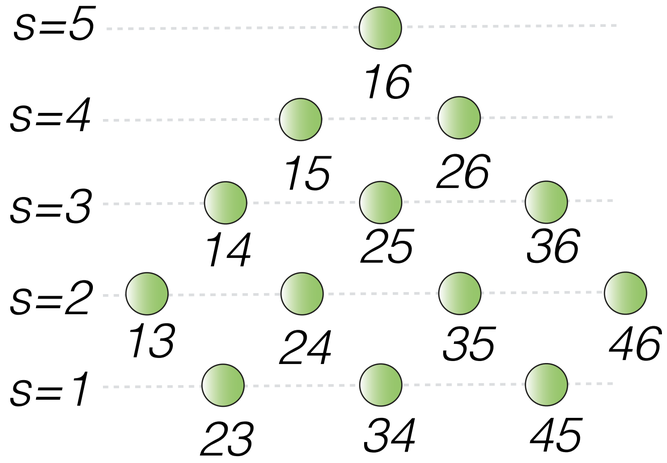

LHZ Architecture: Summary

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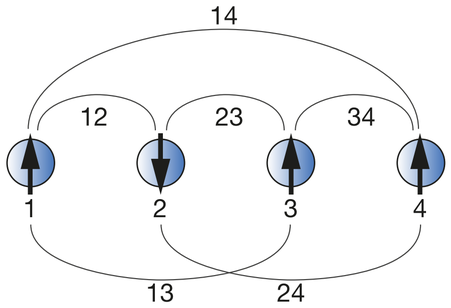
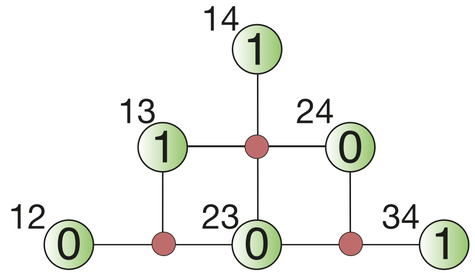
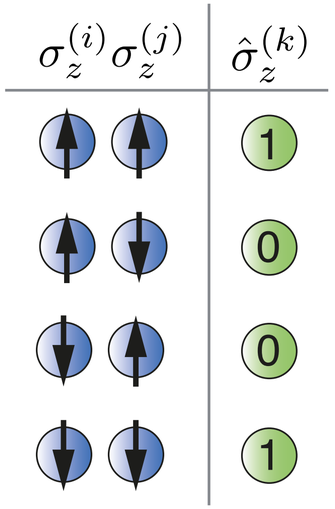




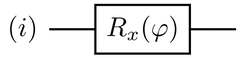
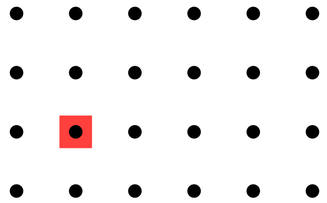
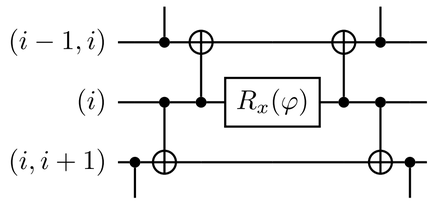
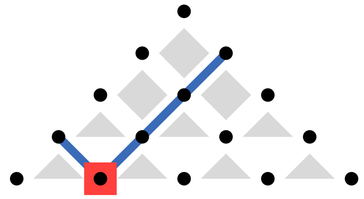
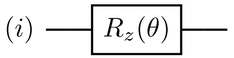
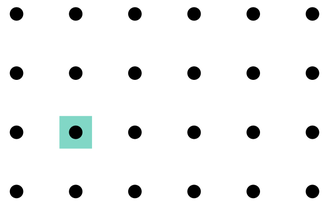
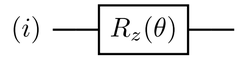
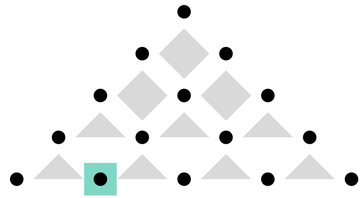
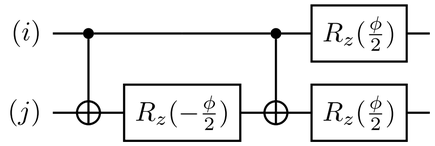
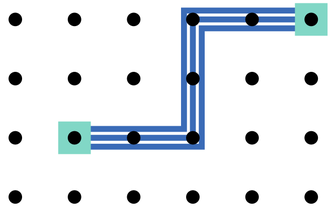
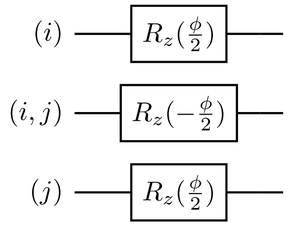
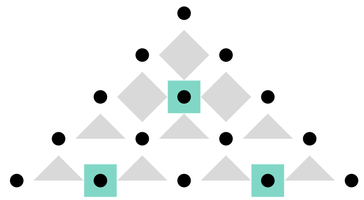


$$H_P = \sum_{i=1}^{N}\sum_{j=1}^{i-1} J_{ij}\sigma_z^{(i)}\sigma_z^{(j)}$$

$$H_{\mathrm{LHZ}} = \sum_{i=1}^{K} J_i\sigma_z^{(i)} + \sum_{l=1}^{K-N+1} -c_l\sigma_z^{(l_1)}\sigma_z^{(l_2)}\sigma_z^{(l_3)}[\sigma_z^{(l_4)}]$$

- The LHZ architecture maps an all-to-all connected spin model to a spin model with only **quasi-local** interactions.
- The physical qubits encode the **parity** of the logical qubits.
- **No long-range interactions** but only local 3- or 4-body couplings are necessary.
- The parity architecture requires nearest-neighbour interactions on a square lattice, **regardless of the qubit platform.**

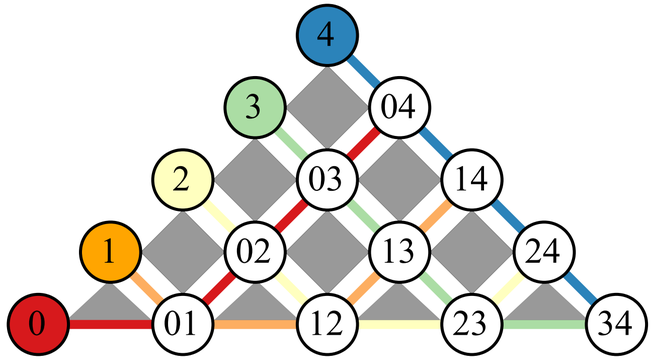
Universal Parity Computing

Gate	Standard Circuit	Schematic Standard Implementation	Circuit in LHZ Scheme	Schematic Implementation in LHZ
$R_x^{(i)}(\varphi)$				
$R_z^{(i)}(\theta)$				
$\mathrm{CP}_{\phi}^{(i,j)}$				

M. Fellner, A. Messinger, K. Ender, and W. Lechner, “Universal Parity Quantum Computing,” Physical Review Letters, vol. 129, no. 18., Oct. 27, 2022. doi: 10.1103/physrevlett.129.180503.

GENERAL SWAP-LESS PARITY METHOD

Computation is generating Parity labels



General method applicable to algorithms based on multi-qubit information processing

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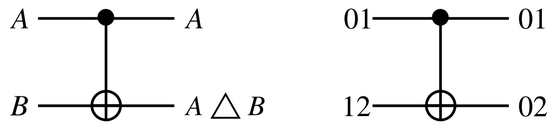

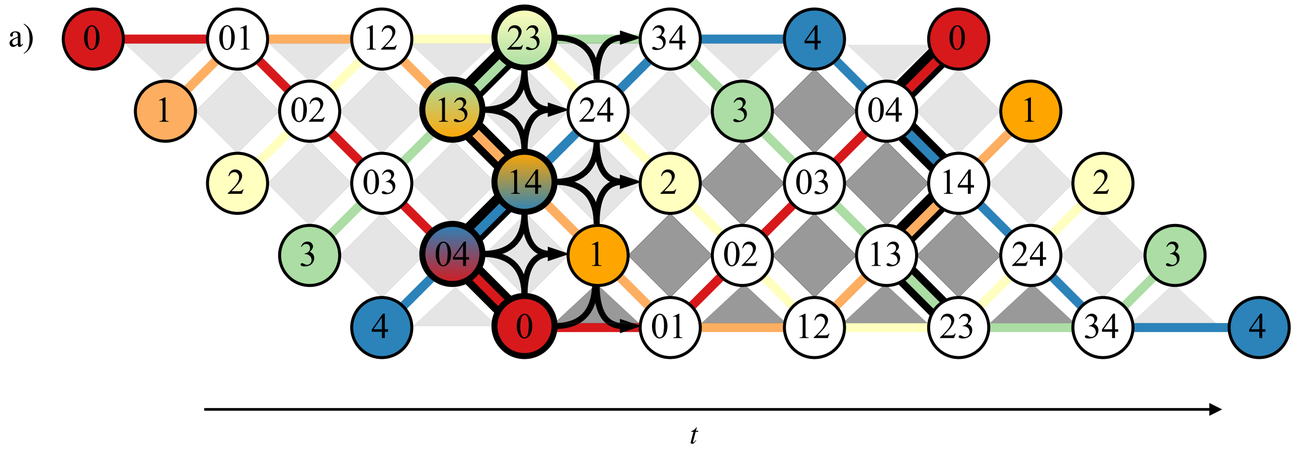

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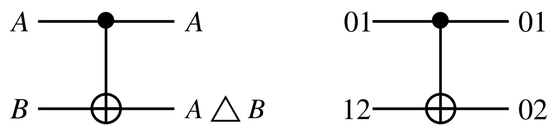

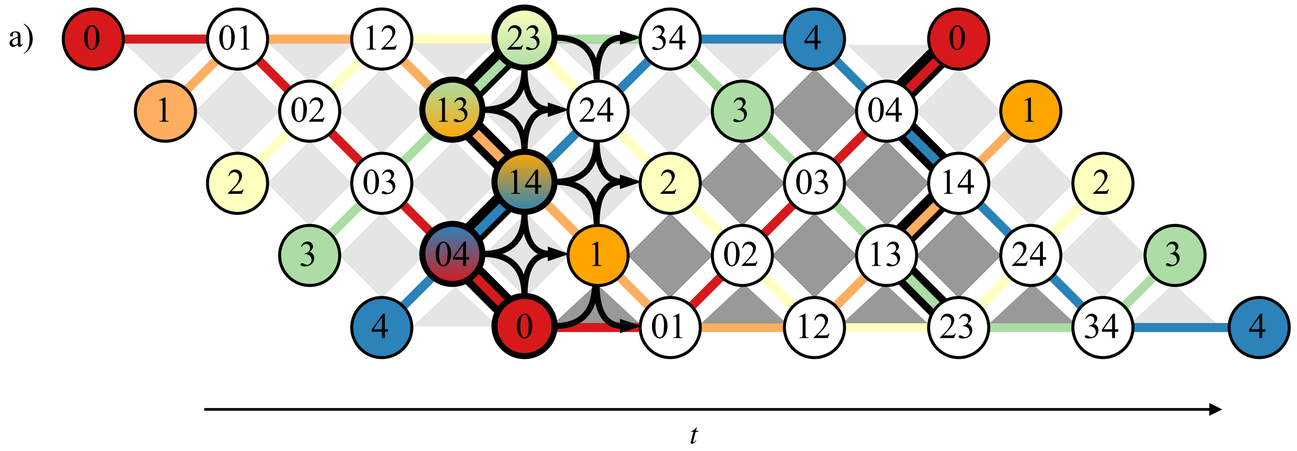

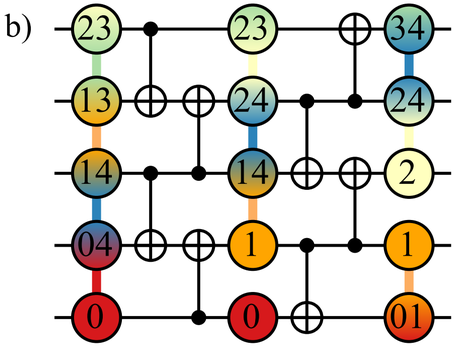

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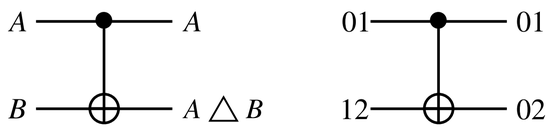

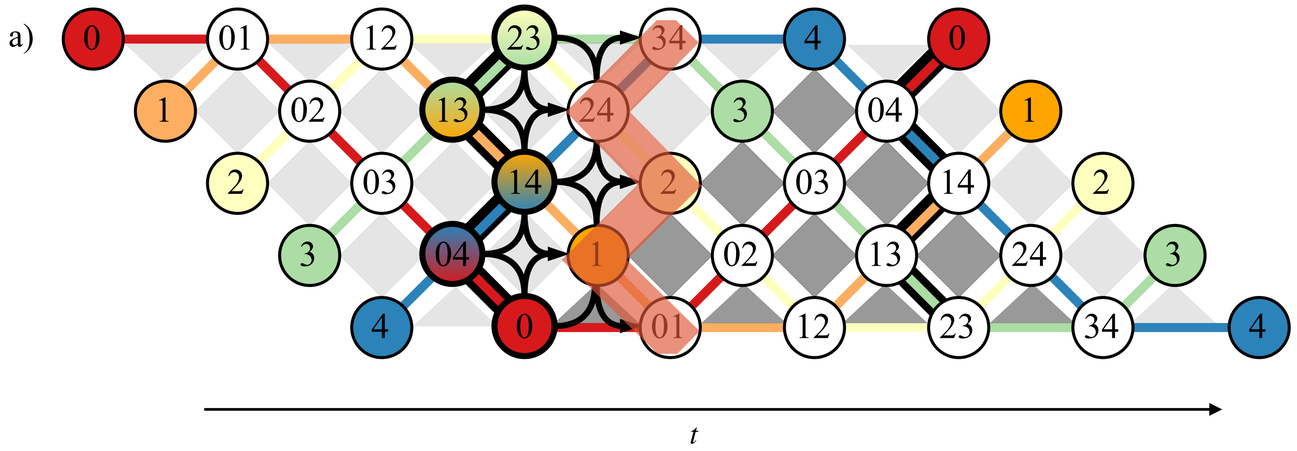

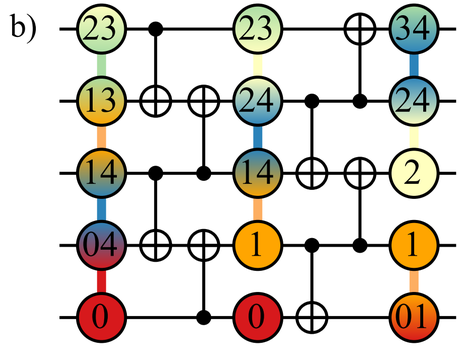

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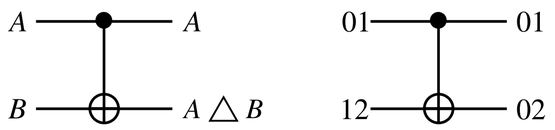

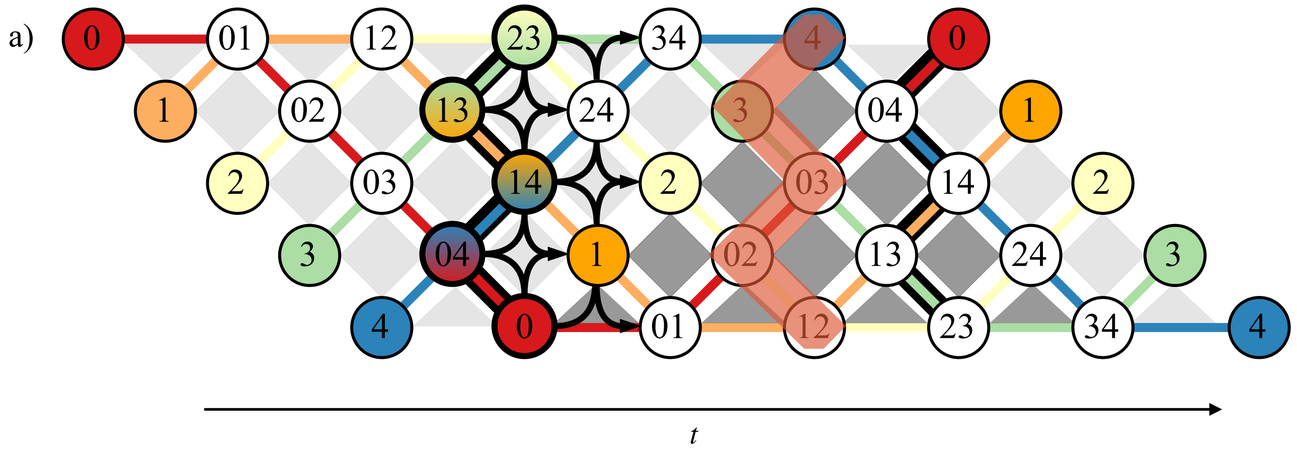

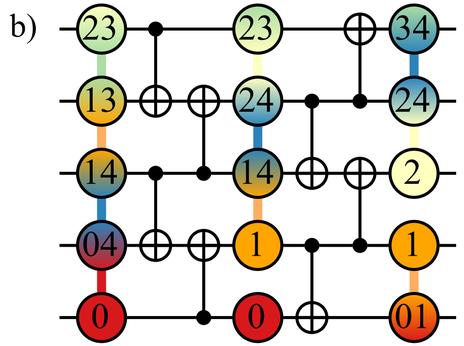

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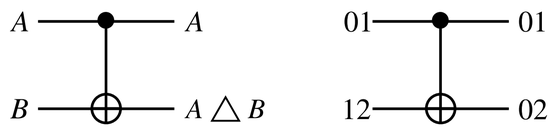

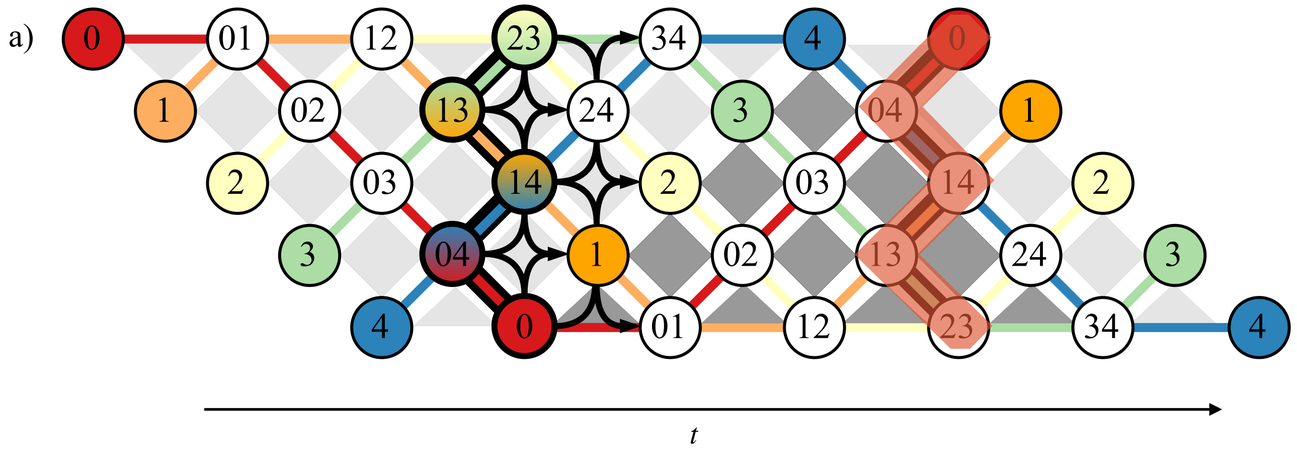

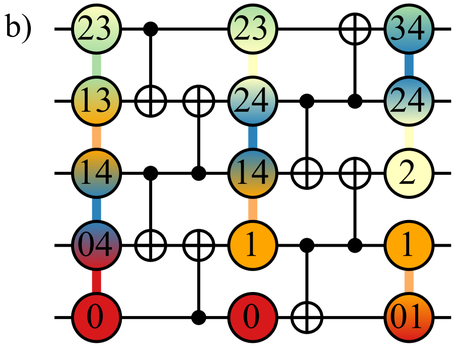

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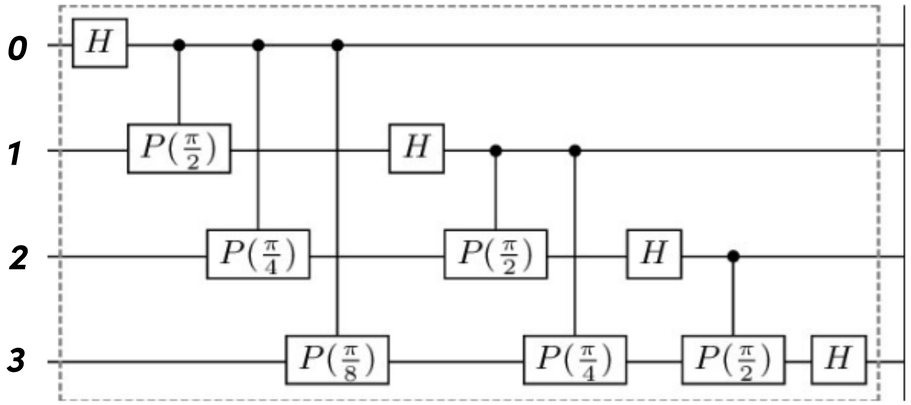
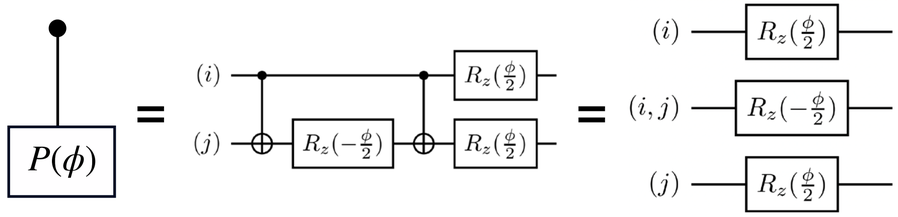
Swap-less parity Quantum Fourier Transform





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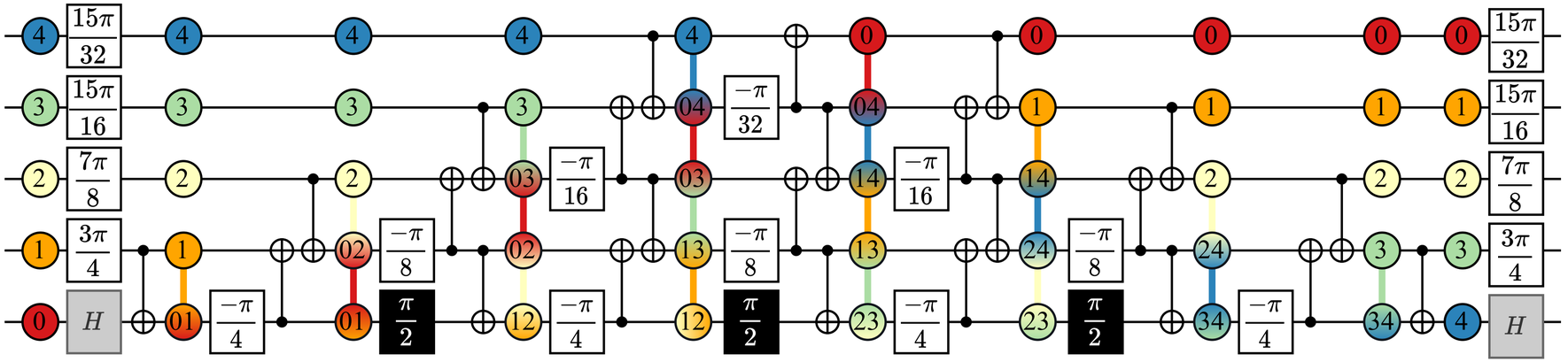
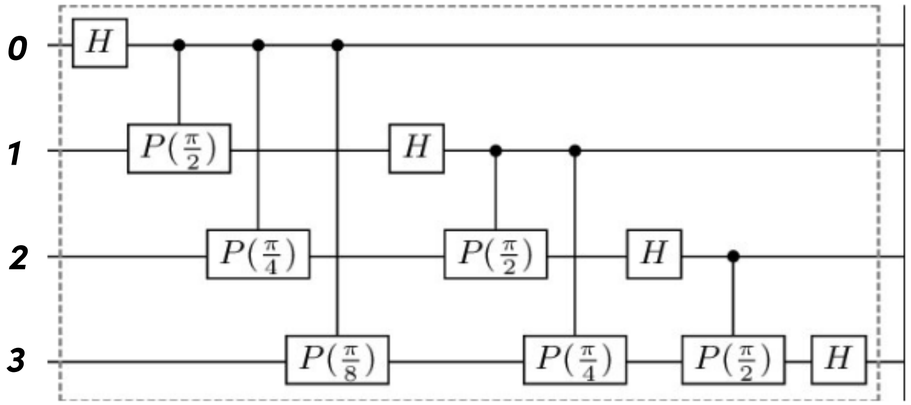
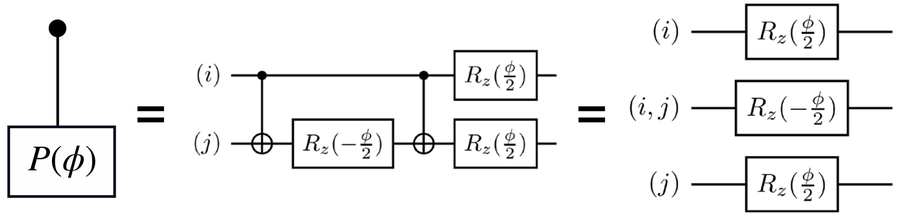




Rx gate

Rz gate



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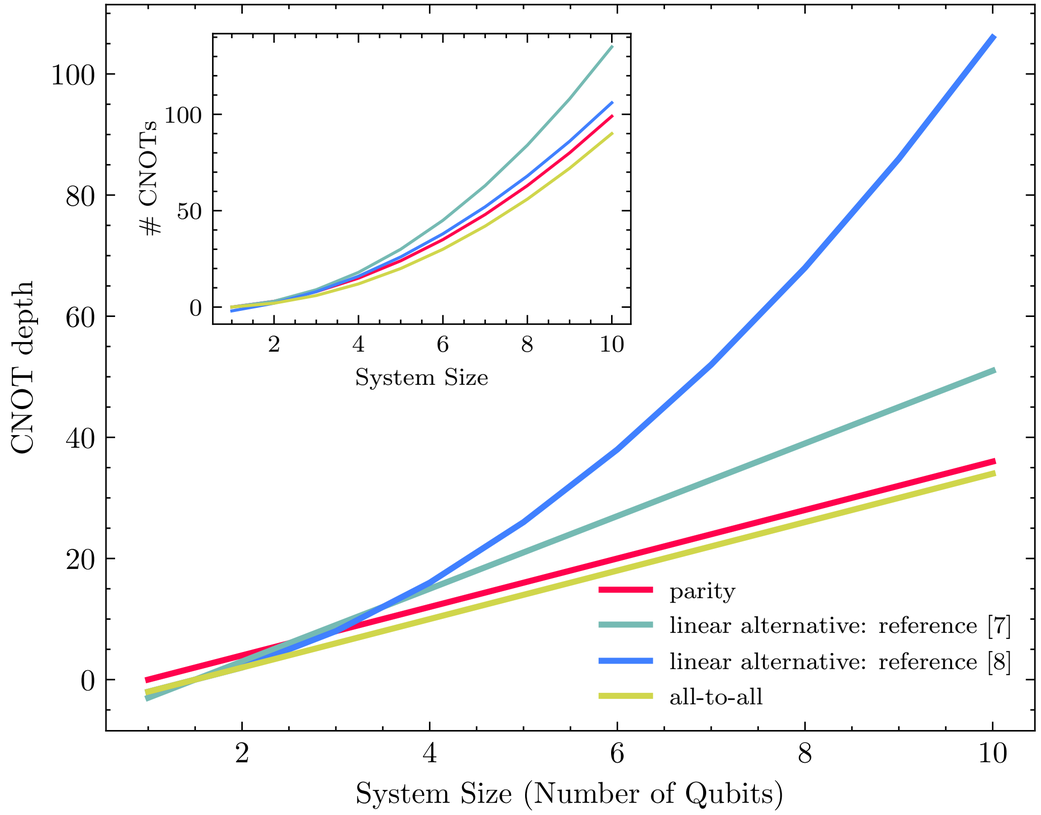
Parity QFT: Scaling

		Optimised gate count	*Optimised depth*	
Resource	Ours	Ref. [8]	Ref. [7]	all-to-all
#CNOTs	n^2-1	n^2+n-4	$\frac{3}{2}n^2-\frac{3}{2}n$	n^2-n
#SQ gates	$\frac{1}{2}n^2+\frac{5}{2}n-2$	$\frac{1}{2}n^2+\frac{5}{2}n-2$	n^2	n^2
total gates	$\frac{3}{2}n^2+\frac{5}{2}n-3$	$\frac{3}{2}n^2+\frac{7}{2}n-6$	$\frac{5}{2}n^2-\frac{3}{2}n$	$2n^2-n$
CNOT depth	$4n-4$	n^2+n-4	$6n-9$	$4n-6$
SQ depth	$n+1$[a]	$2n+1$	$4n-4$	$4n-4$
total depth	$5n-3$	n^2+3n-3	$10n-13$	$8n-10$



[7] A. Holmes, et al., Quantum Sci. Technol. **5**, 025009 (2020)
[8] B. Park, D. Ahn, Sci. Rep. **13**, 8638 (2023)

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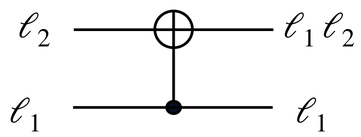
Parity Twine Chain

Goal: implement all 2-body labels

CNOTs can be used to encode labels



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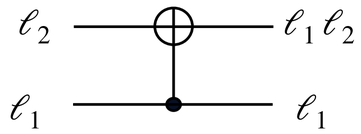
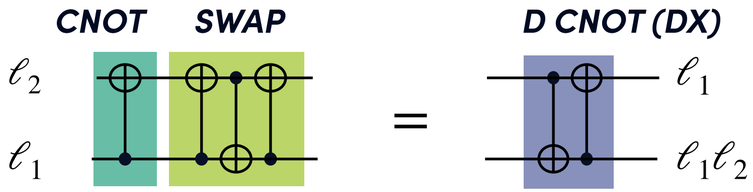


Encode 2-body labels that contain ℓ_1



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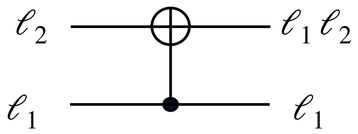

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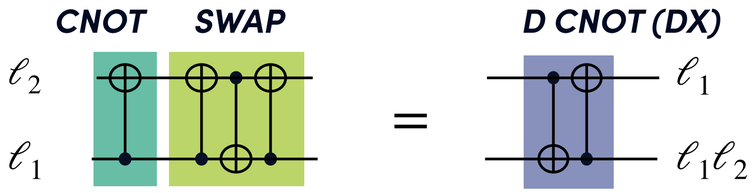
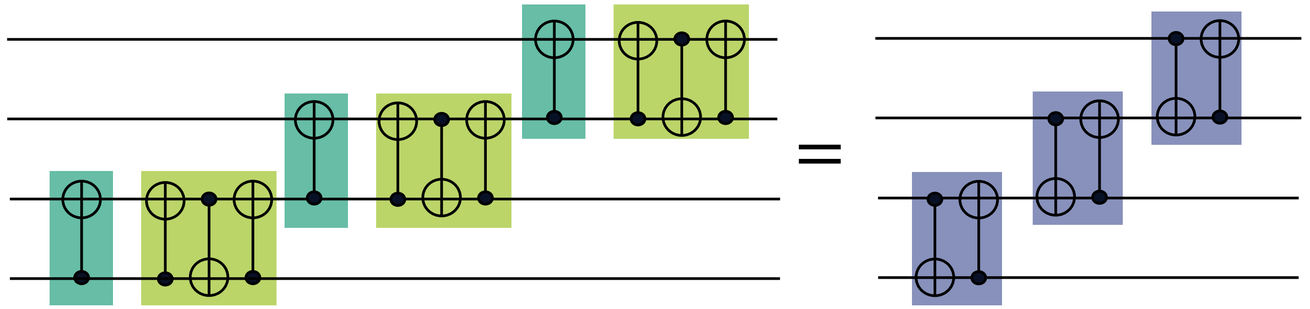
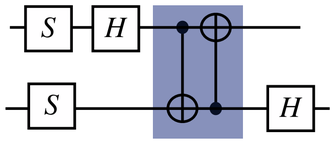


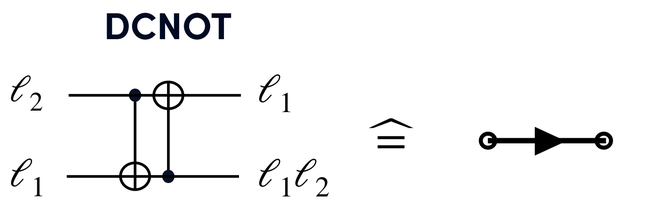
Parity Twine chain



iSWAP



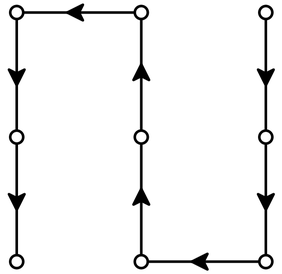
Parity Twine: Square Grid



≙

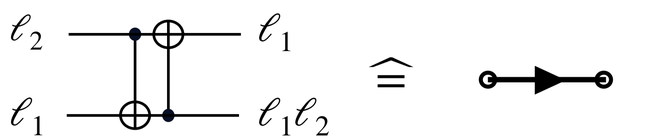
“backbone”

only backbone



Parity Twine: Square Grid

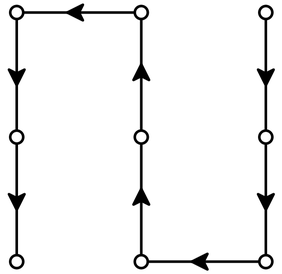
DCNOT



≙

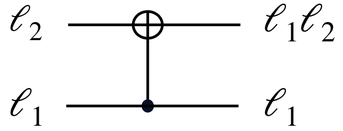
“backbone”

only backbone



Due to increased connectivity we don’t always need a DCNOT!

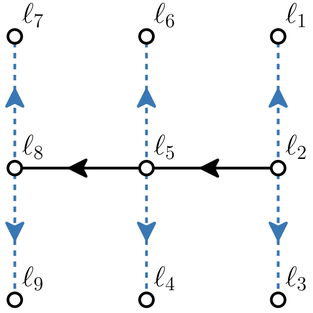
CNOT



≙

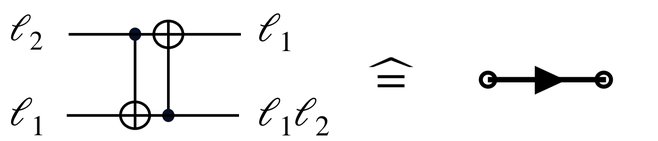
“legs”

backbone and legs



Parity Twine: Square Grid

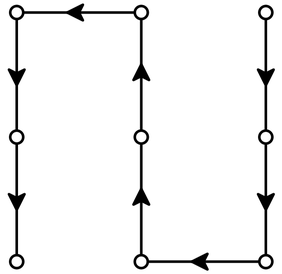
DCNOT



$\widehat{=}$

“backbone”

only backbone



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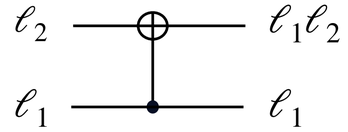
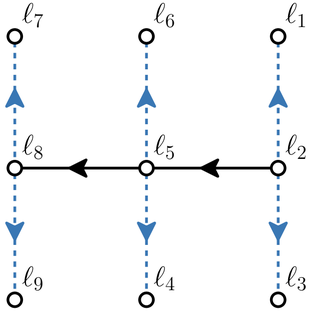
CNOT

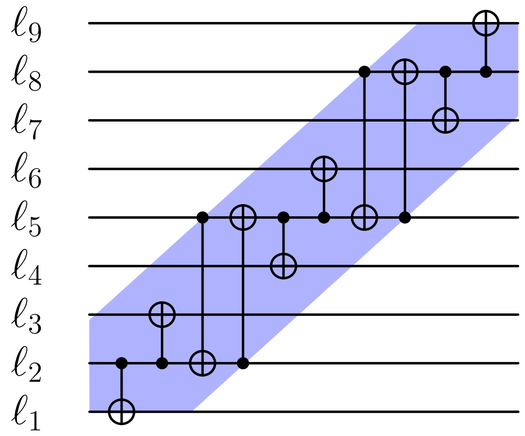


$\widehat{=}$

“legs”

backbone and legs





Square Grid Parity Twine Chain

Saves $\frac{1}{3}$ ***of gates compared to LNN***

LNN: n^2 → ***Square grid:*** $\frac{2}{3}n^2$

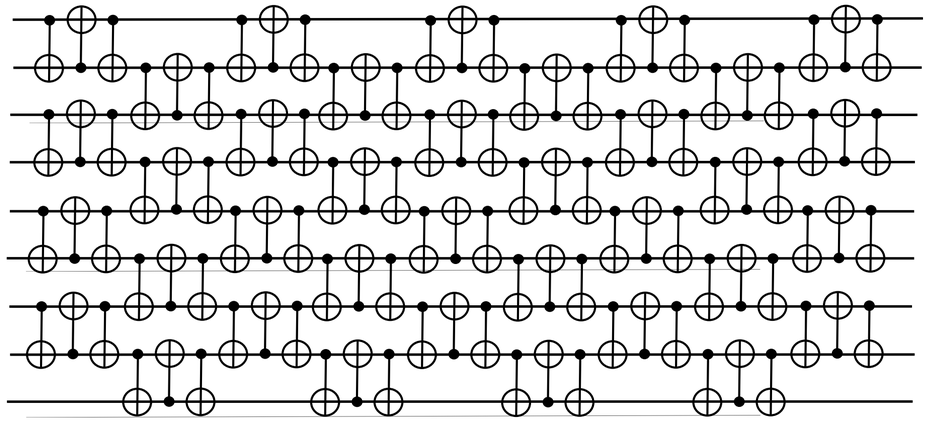
Previous conjecture:

No advantage compared to linear connectivity!

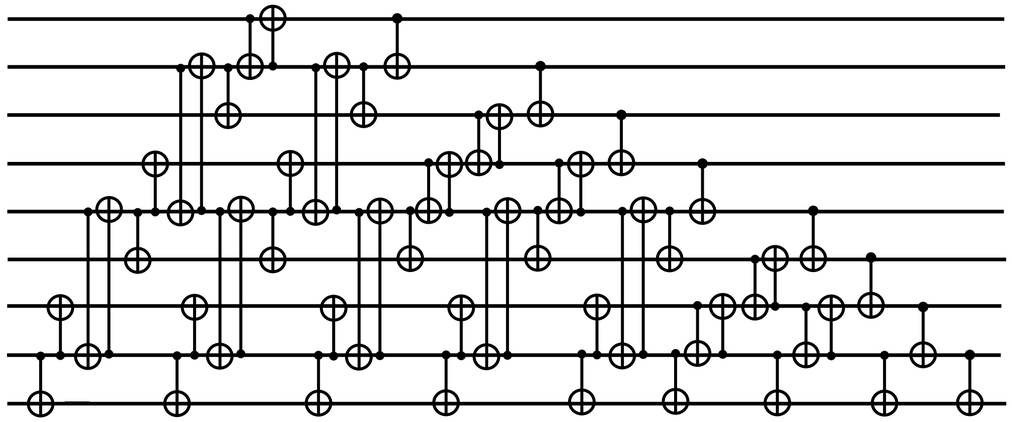
J. Weidenfeller et al., Quantum 6, 870 (2022)

Parity Twine: Square Grid

State of the art: SWAP networks



Parity Twine

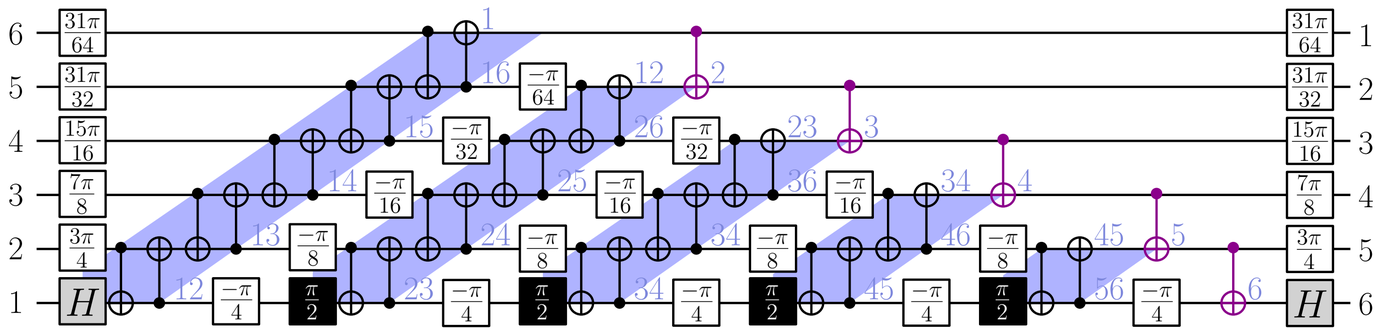


Square grid

Quantum Fourier Transform

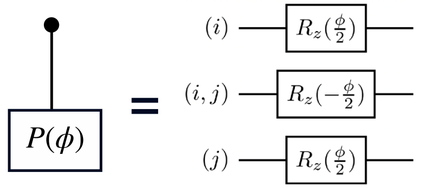
$$U_{\mathrm{QFT}} = \prod_{i=1}^{n} \left[H^{(i)} \prod_{j=i+1}^{n} \mathrm{CP}^{(i,j)}_{j-i+1} \right] \quad \textit{with} \quad P_k \equiv \begin{pmatrix} 1 & 0 \\ 0 & e^{2\pi i/2^k} \end{pmatrix}.$$

Linear Chain



$\theta = R_X(\theta)$

$\theta = R_Z(\theta)$



$$H = R_z(\pi/2)R_x(\pi/2)R_z(\pi/2)$$

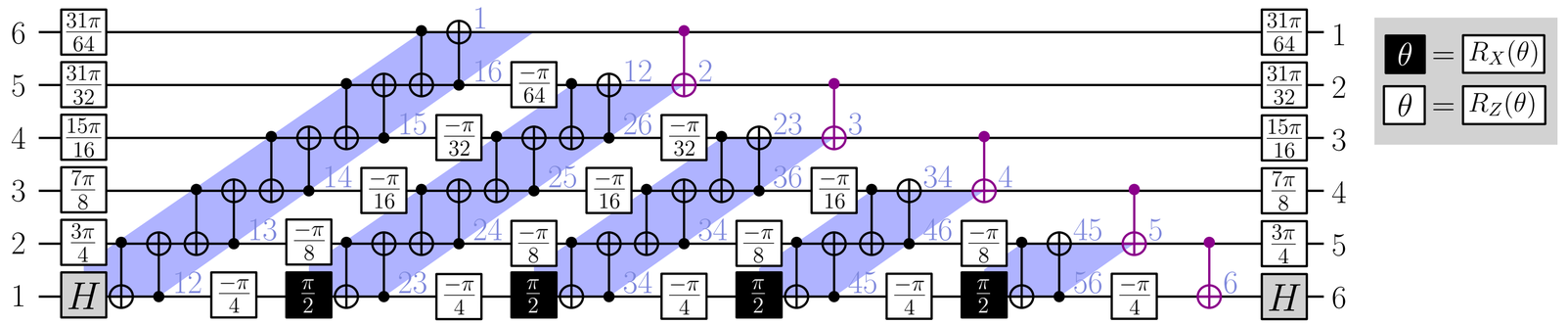
B. Klaver, S. Rombouts, M. Fellner, A. Messinger, Ki. Ender, K. Ludwig, and W. Lechner, arXiv:2408.10907 (2024)

F. Dreier, C. Fleckenstein, G. Aigner, M. Fellner, R. Stahn, M. Lanthaler, and W. Lechner, arXiv:2501.14020 (2025)

Quantum Fourier Transform

$$U_{\mathrm{QFT}} = \prod_{i=1}^{n} \left[H^{(i)} \prod_{j=i+1}^{n} \mathrm{CP}_{j-i+1}^{(i,j)} \right] \quad \textit{with} \quad P_k \equiv \begin{pmatrix} 1 & 0 \\ 0 & e^{2\pi i/2^k} \end{pmatrix}.$$

Linear Chain



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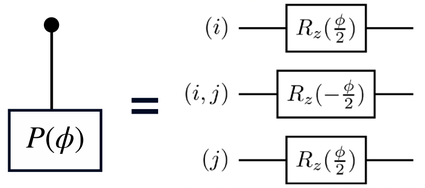
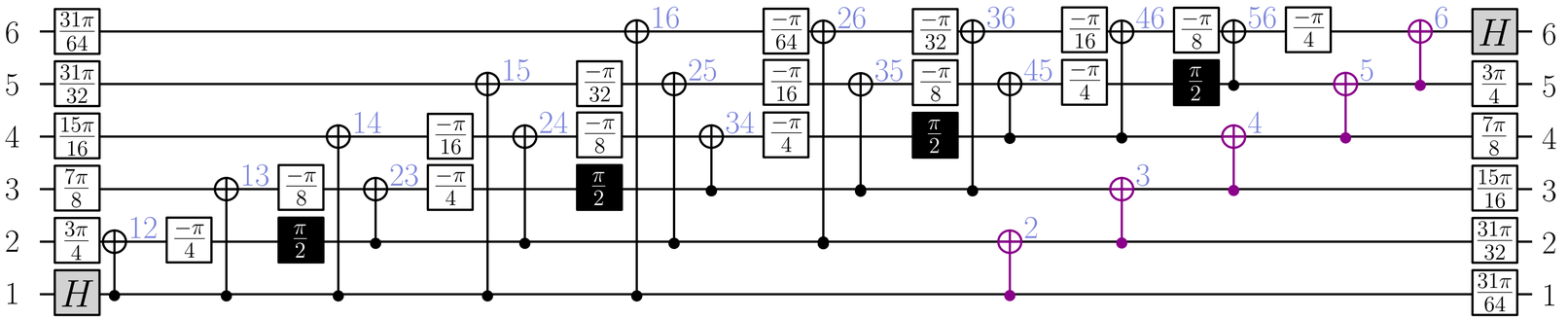


$$H = R_z(\pi/2)R_x(\pi/2)R_z(\pi/2)$$

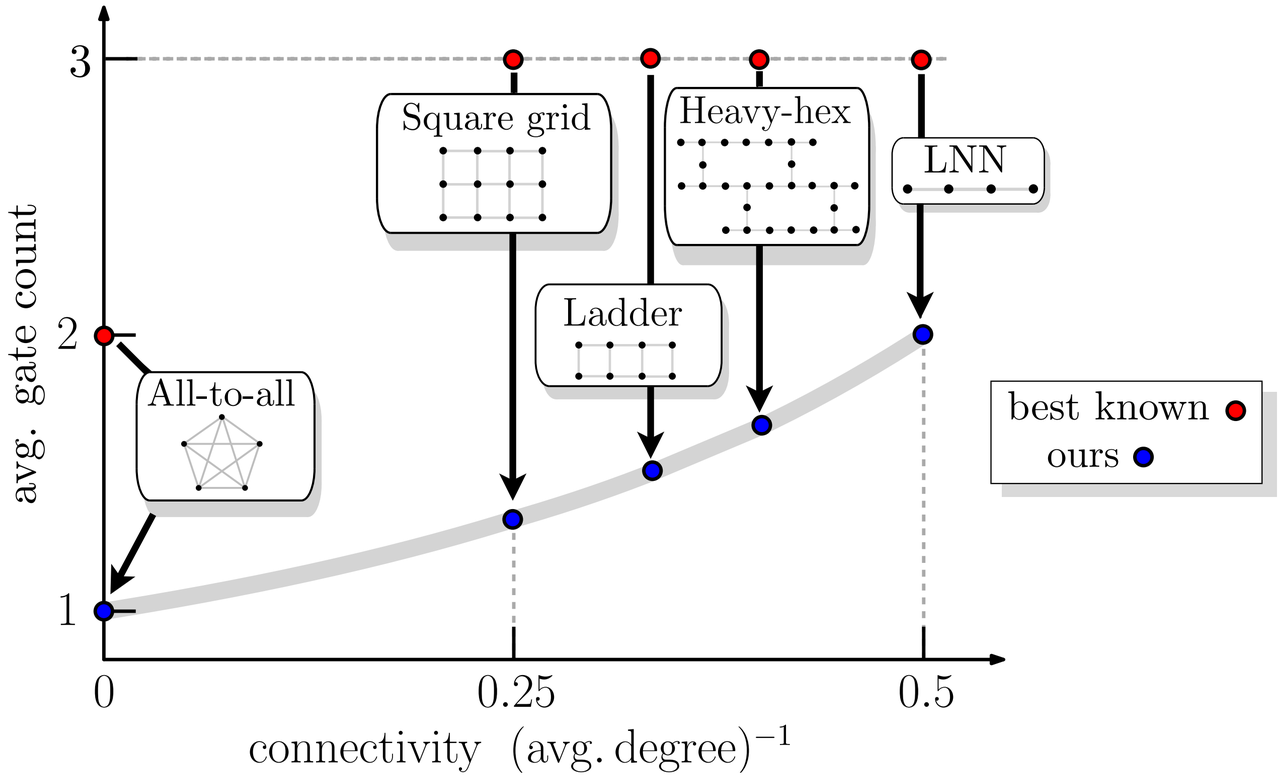
All-to-all



B. Klaver, S. Rombouts, M. Fellner, A. Messinger, Ki. Ender, K. Ludwig, and W. Lechner, arXiv:2408.10907 (2024)

F. Dreier, C. Fleckenstein, G. Aigner, M. Fellner, R. Stahn, M. Lanthaler, and W. Lechner, arXiv:2501.14020 (2025)

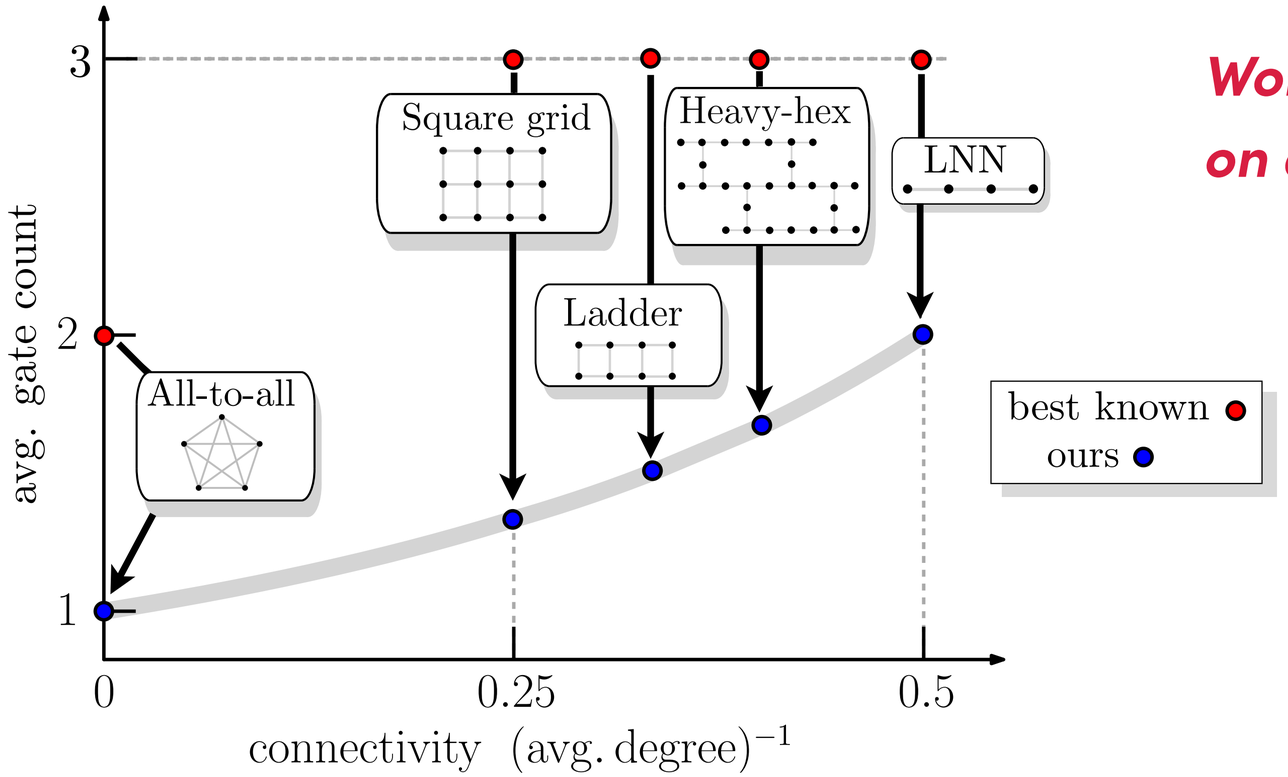
Parity Twine



Connectivity graph	QFT ours				QFT best known (count-optimized) [16]				QFT best known (depth-optimized) [40]			
	count	depth	μ	ν	count	depth	μ	ν	count	depth	μ	ν
LNN	n^2	$4n$	2	4	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
heavy hexagon	$\frac{5}{6}n^2$	$5n$	$1+\frac{2}{3}$	5	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
ladder	$\frac{3}{4}n^2$	$3n$	$1+\frac{1}{2}$	3	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
square grid	$\frac{2}{3}n^2$	$6n$	$1+\frac{1}{3}$	6	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
all-to-all	$\frac{1}{2}n^2$	$2n$	1	2	n^2	$4n$	2	4	n^2	$4n$	2	4

F. Dreier, C. Fleckenstein, G. Aigner, M. Fellner, R. Stahn, M. Lanthaler, and W. Lechner, arXiv:2501.14020 (2025)

Parity Twine

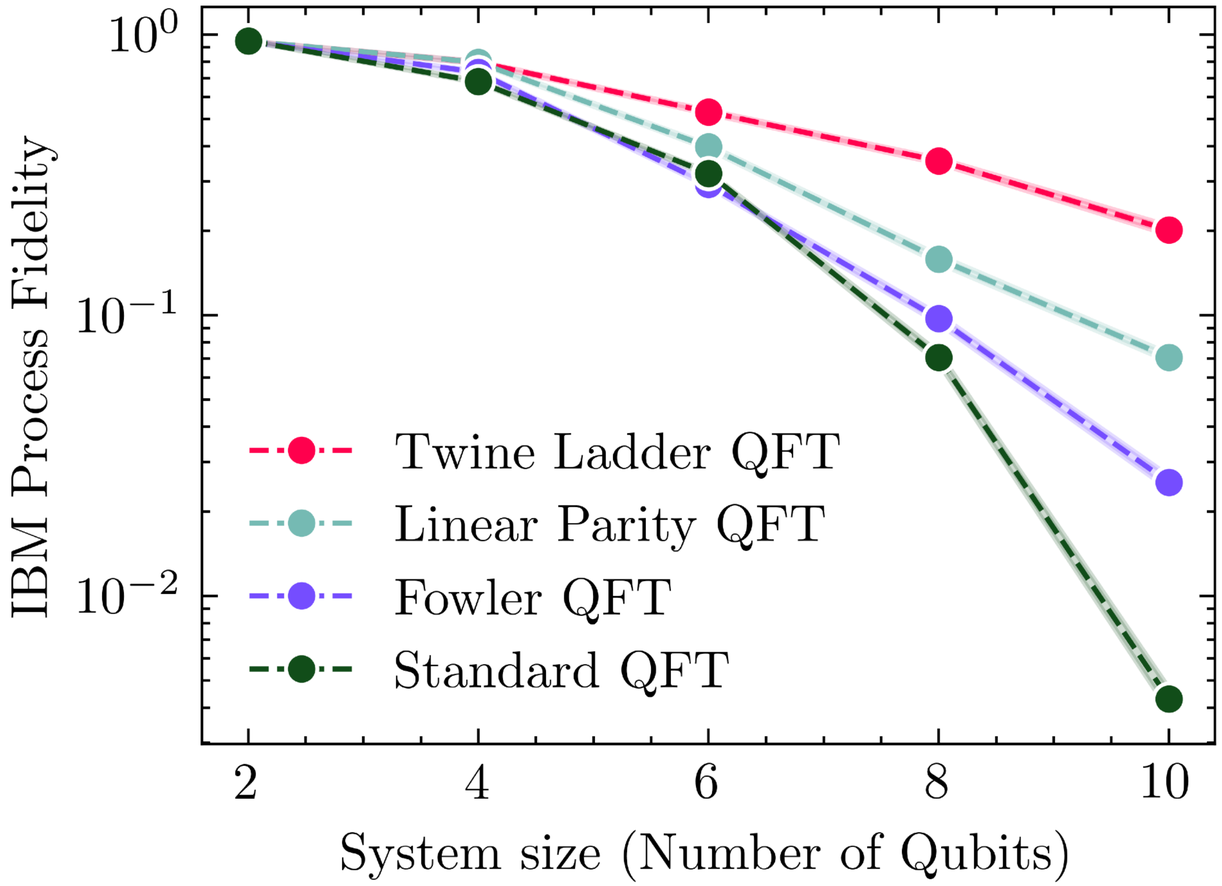


World-record on all geometries.

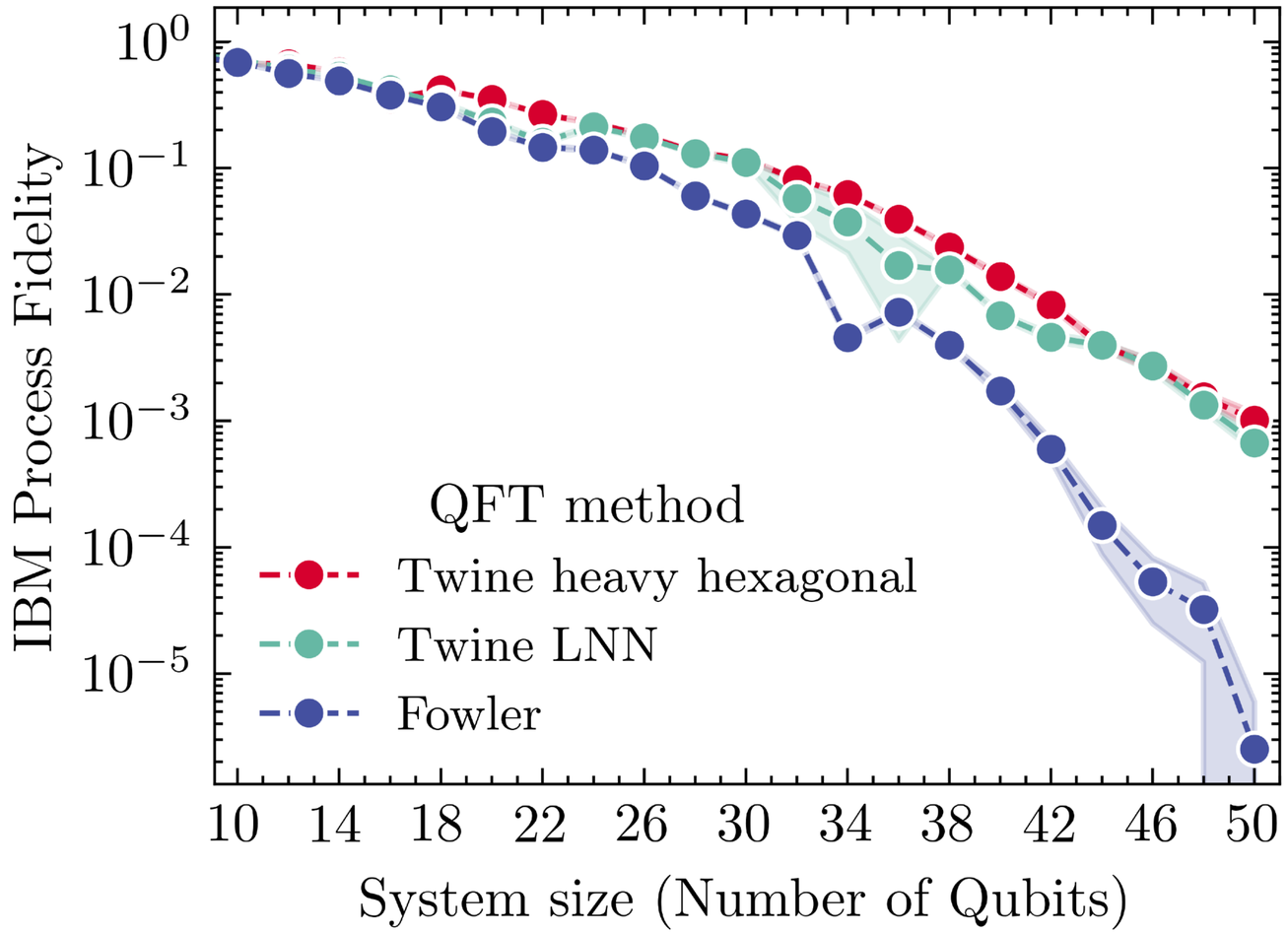
Connectivity graph	QFT ours				QFT best known (count-optimized) [16]				QFT best known (depth-optimized) [40]			
	count	depth	μ	ν	count	depth	μ	ν	count	depth	μ	ν
LNN	n^2	$4n$	2	4	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
heavy hexagon	$\frac{5}{6}n^2$	$5n$	$1+\frac{2}{3}$	5	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
ladder	$\frac{3}{4}n^2$	$3n$	$1+\frac{1}{2}$	3	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
square grid	$\frac{2}{3}n^2$	$6n$	$1+\frac{1}{3}$	6	n^2	n^2	2	n	$\frac{3}{2}n^2$	$6n$	3	6
all-to-all	$\frac{1}{2}n^2$	$2n$	1	2	n^2	$4n$	2	4	n^2	$4n$	2	4

F. Dreier, C. Fleckenstein, G. Aigner, M. Fellner, R. Stahn, M. Lanthaler, and W. Lechner, arXiv:2501.14020 (2025)

Hardware realization (IQM Device)



Hardware realization (IBM Heron)



General Compilation

Optimizing QAOA circuit transpilation with parity twine and SWAP network encodings

J. A. Montañez-Barrera*, Yanjun Ji†, Michael R. von Spakovsky ‡, David E. Bernal Neira‖, Kristel Michielsen*§¶
*Institute for Advanced Simulation
Jülich Supercomputing Centre, Forschungszentrum Jülich 52425 Jülich, Germany
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***Abstract*—Mapping quantum approximate optimization algorithm (QAOA) circuits with non-trivial connectivity in fixed-layout quantum platforms such as superconducting-based quantum processing units (QPUs) requires a process of transpilation to match the quantum circuit on the given layout. This step is critical for reducing error rates when running on noisy QPUs. Two methodologies that improve the resource required to do such transpilation are the SWAP network and parity twine chains (PTC). These approaches reduce the two-qubit gate count and depth needed to represent fully connected circuits. In this work, a simulated annealing-based method is introduced that reduces the PTC and SWAP network encoding requirements in QAOA circuits with non-fully connected two-qubit gates. This method is benchmarked against various transpilers and demonstrates that, beyond specific connectivity thresholds, it achieves significant reductions in both two-qubit gate count and circuit depth, surpassing the performance of Qiskit's transpiler at its highest optimization level. For example, for a 120-qubit QAOA instance with 25% connectivity, our method achieves an 85% reduction in depth and a 28% reduction in two-qubit gates. Finally, the practical impact of PTC encoding is validated by benchmarking QAOA on the `ibm_fez` device, showing improved performance up to 20 qubits, compared to a 15-qubit limit when using SWAP networks.**

***Index Terms*—Parity Twine Chain, QAOA, Weighted MaxCut, ibm_fez, Quantum Circuit Transpilation, SWAP Networks**

(nondeterministic polynomial-time) complete [4]. Therefore, efficient heuristic transpilation that minimizes the number of gates needed is essential for executing algorithms on near-term quantum devices. Connectivity constraints are typically addressed by inserting SWAP gates, which introduce significant noise since two-qubit gates such as CNOT or CZ gates are the most dominant sources of error [5], and a single SWAP gate is typically decomposed into three CNOT gates.

A common technique for representing a fully connected circuit using a 1D chain of qubits layout is known as the SWAP network strategy [6]–[11]. It applies SWAP gates between neighboring pairs in a brickwork pattern. At each time step, the logical qubits are moved around, creating temporal connections between them. A recent novel approach is the use of parity twine chains (PTC) [12], [13]. This method has shown a reduction in the number of two-qubit gates and circuit depth needed to encode the quantum approximate optimization algorithm (QAOA) [14] and the quantum Fourier transform [15], [16].

In this work, PTC and SWAP encodings are compared against selected transpilation frameworks, including the Qiskit transpiler with optimization level 3 (Qiskit-T), IBM Quan-

optimization level. For example, for a 120-qubit QAOA instance with 25% connectivity, our method achieves an 85% reduction in depth and a 28% reduction in two-qubit gates. Finally, the practical impact of PTC encoding is validated by benchmarking

Conclusion

Parity Architecture

Efficient general algorithm embedding on **any hardware layout**

—

World-Record **Synthesis of Quantum Algorithms**
Reduced circuit **depth** and **gate count**
and **improved process fidelity**
without measurement or post-processing